Analysis and Loss Measurements of WBG-Based Devices

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Abstract:
Commercial power supplies with wide-bandgap (WBG) Technology promise enhanced efficiency. PECTA analyzes WBG-based devices, supported by Swiss research, focusing on measurement concepts, loss assessments, and a deep understanding of the WBG device benefits. The POWERlab at EPFL works on efficient WBG semiconductor technologies and develops accurate electrical measurement methods to provide insights into loss sources. In addition, calorimetric techniques ensure precise efficiency evaluations, vital for high-frequency comparisons. This foundational work guides standardization efforts, fostering collaboration with industry and standardization bodies. These initial steps pave the way for improved efficiency measurements and the promotion of WBG technologies.

About the IEA 4E Power Electronic Conversion Technology Annex (PECTA):
Power electronic devices incorporating Wide Band Gap (WBG) technologies are maturing rapidly and offer enormous opportunities for improved energy efficiency. 4E´s PECTA assesses the efficiency benefit of utilizing the emerging WBG technology, keeps participating countries informed as markets for Wide Band Gap technologies devices develop, and engages with research, government and industry stake-holders worldwide to lay the base for suitable policies in this area.

Further information on PECTA is available at:
https://pecta.iea-4e.org.

About the IEA Implementing Agreement on Energy Efficient End-Use Equipment (4E):
The Technology Collaboration Programme on Energy Efficient End-Use Equipment (4E TCP), has been supporting governments to co-ordinate effective energy efficiency policies since 2008. Fourteen countries and one region have joined together under the 4E TCP platform to exchange technical and policy information focused on increasing the production and trade in efficient end-use equipment. However, the 4E TCP is more than a forum for sharing information: it pools resources and expertise on a wide a range of projects designed to meet the policy needs of participating governments. Members of 4E find this an efficient use of scarce funds which results in outcomes that are far more comprehensive and authoritative than can be achieved by individual jurisdictions. The 4E TCP is established under the auspices of the International Energy Agency (IEA) as a functionally and legally autonomous body.
Current members of 4E TCP are: Australia, Austria, Canada, China, Denmark, European Commission, France, Japan, Korea, Netherlands, New Zealand, Switzerland, Sweden, UK and USA.

The main collaborative research and development activities under 4E include the

- Electric Motor Systems Annex (EMSA)
- Solid State Lighting (SSL) Annex
- Electronic Devices and Networks Annex (EDNA)
- Power Electronic Conversion Technology Annex (PECTA)

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Executive Summary

First commercial power supplies (SMPS = Switched Mode Power Supply) with incorporated Wide-bandgap (WBG) Technology are available on the market. WBG technology offers an enormous potential to increase the efficiency of these products

Cofounded by the Swiss Federal Office of Energy (SI 502100-01) PECTA analyzed existing WBG-based devices in terms of efficiency (or equivalently losses) in comparison with conventional Si-based technology. This activity includes mainly the thorough and detailed elaboration of measurement concepts, loss measurements, and analyzing additional and particular benefits of the WBG-based devices (part 1).

On a lower level, the information on the loss mechanisms of commercially available devices opens opportunities to improve their design right at the semiconductor level. The POWERlab at EPFL has extensive expertise in the design and fabrication of the next generation of power devices, having proposed several novel WBG semiconductor technologies for more efficient power devices. The information on the existing sources of losses in available WBG semiconductor devices will be of huge value for the design of new technologies to mitigate this effect. In close collaboration with the appropriate industry, such information shall be converted into possible technologies for more efficient future devices.

In addition to common electrical measurements, the use of calorimetric techniques to measure losses enables a much more precise determination of the efficiency of devices and systems. This is particularly important when comparing different devices and systems at higher switching frequencies, since electrical measurements are subject to spurious errors due to bandwidth limitations, delay mismatches between the current and voltage probes, loading effects, and electromagnetic interference.

On a higher level, this basic work on the proper measurement of losses will offer guidelines to standardize measurements among different technologies, enabling a fair comparison of the results to the existing norms. The idea is to establish initial relationships with companies and standardization bodies/Organizations to discuss any deviation observed between the results, aiming to cross the information between different methods and standards. With these initial steps the basic guidelines for a better standardization of efficiency measurements will be established, supporting a proper promotion of WBG technologies.

Contents

1. Introduction

1.1. Overview and Objectives

PECTA is interested in a standardized definition of efficiency performance, the proper and reproducible measurement of losses and the proper definition of efficiency classification of wide-bandgap (WBG) semiconductor devices and at a later stage even appliances. The ultimate goal is to provide efficiency and performance standards for WBG devices. These standards will allow WBG devices to be characterized and compared in an internationally accepted and technically appropriate manner. This work on the proper determination of losses by accurate measurement will offer guidelines to standardize measurements between different technologies, enabling a fair comparison of results with existing norms. The principal idea is to establish initial relationships with companies and standardization bodies/organizations to discuss any discrepancies between the results, aiming to compare and put into proper relation the information between different methods and standards. With these initial steps the basic guidelines for a proper and elaborated method of efficiency measurements as a base for standardization will be established, supporting a proper promotion of WBG technologies.

1.2. Background

Electricity is the fastest-growing form of end-use energy [1], making energy efficiency a key approach to decoupling the energy demand for economic growth from an increase in carbon dioxide emissions [2]. Power electronics, which rely on power semiconductors, are responsible for controlling and converting electrical power in the most adapted form for transmission, distribution, and end-user consumption. However, more than 10% of the electricity consumed in the world is wasted in power conversion, which exceeds the entire supply of current solar and wind energies [3]. Efficient power conversion offers a low-cost energy resource to meet future energy demands, reduce carbon dioxide emissions, and enable the concurrent development of renewable energy technologies [4],[5].

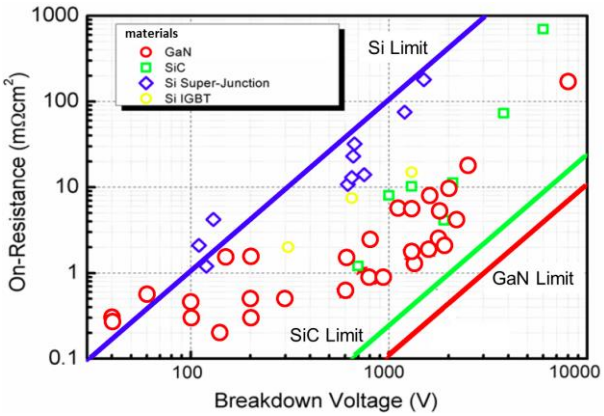

Fig. 1 Specific on-resistance versus Breakdown voltage for SiC, GaN and Si super-junctions power devices. Theoretical curves for Si, SiC and GaN.

Wide-band-gap semiconductors, such as SiC and GaN, offer inherent advantages for high-efficiency power-electronic devices. Their excellent electronic properties, such as large breakdown fields, result in a Baliga's Figure of Merit [6] much larger than in conventional Silicon-based devices. The high electron mobility and low on-state resistance of GaN semiconductors enable higher efficiency at a smaller size and a much higher operating frequency, which can lead to a huge reduction in the entire power converter system.

In addition to higher efficiencies, another main motivation for the adoption of GaN is the possibility of much more compact systems and even integrated power chips. This is mainly due to its ability to switch large voltages and currents at very high frequencies, in the MHz range. This enables a significant reduction of the entire power converter, since the size of the energy storage elements, such as capacitors and inductors are, to a large extent, inversely proportional to the switching frequency, resulting in very large power density systems.

However, today's GaN devices have challenges both in their static and dynamic performances. First, the current performance of these devices, in terms of on-state resistance (R_{ON}) versus area (A) and breakdown voltage (VBR), is still far from the fundamental limits of these materials (Fig. 1). Unlike in SiC and Si vertical devices, a major drawback of these lateral devices is the non-uniform electric field distribution in the depletion region formed between the source and drain terminals, which severely limits the useful portion of the access region that can hold large off-state voltages. This requires very special field plate structures to manage the high electric field. In addition, the current flows through a single highly-conductive channel very near the device surface, making the on-state performance extremely prone to surface traps. This significantly affects the switching performance of GaN devices through the degradation of their dynamic on-resistance. In other words, the resistance of the device increases when it is switching compared to its static resistance. Fig. 2 gives a general summary of the multiple technologies present in typical GaN devices. It is worth noticing that GaN devices from different vendors can be based on very distinct device architectures, that may significantly affect their switching performance. For instance, while power switches require normally-OFF (enhancement (E)-mode) characteristics, GaN HEMTs are normally-on devices (depletion (D)-mode), due to the large electron density present in the 2DEG at the AlGAN/GaN interface. This issue can be bypassed with a cascode configuration [7] that realizes the normally-OFF operation at a circuit level, by matching and connecting a high-voltage normally-ON GaN MISHEMT to a low-voltage normally-OFF Si MOSFET. The cascode approach avoids the complex engineering of the gate region, providing a robust MOS gate that has large positive VTH and can be controlled as in conventional Si MOSFETs. This approach, however, requires an extra Silicon transistor that may hinder some of the potential of the GaN [8], particularly for future integrated power circuits. A very common technology relies on p-type material deposited over the gate region [9]–[14], such as p-GaN, p-AlGaN or p-InGaN. This raises the conduction band below the gate electrode, depleting this region of electrons and resulting in positive threshold voltages [15], [16]. The p-GaN technology enables true normally-OFF devices, offering better control of the slew rate and more flexibility for the users [8]. However, the maximum gate voltage is also limited due to the common absence of the gate insulator as the gate "diode" turns on which makes the device quite vulnerable and requires complicated driving circuits for gate protection, degrading the reliability of the conversion system.

As it will be shown in this report, these different technologies to achieve e-mode operation have a significant impact on the device performance at high switching frequencies. Therefore, it is important to carefully characterize the specific behaviors of different GaN device architectures to ensure maximum efficiency at a circuit level.

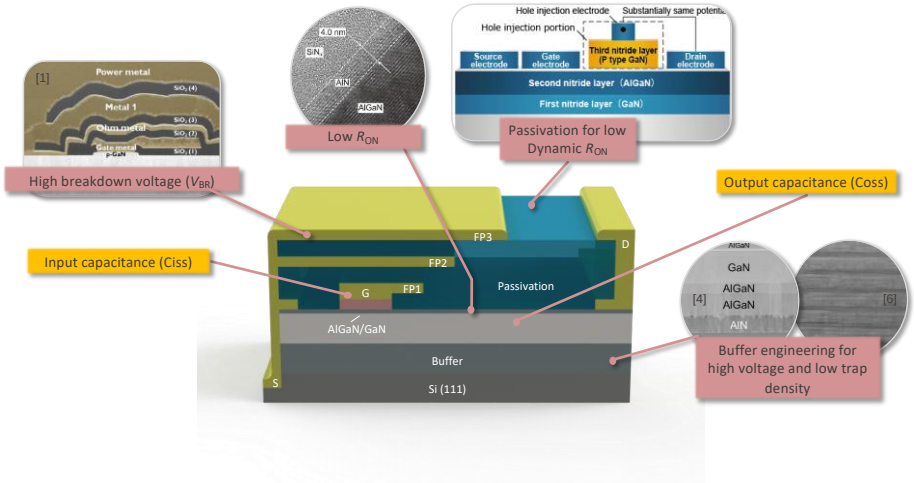

Fig. 2 Schematic of a GaN power device, showing some of the main technologies involved on a device level. In addition, this schematic highlights two important aspects of a power device: input and output capacitances.

2. OFF-State Losses: The Role of Output Capacitance

Within our research efforts, we have found that the device Output Capacitance (C_O) is one of the key device characteristics that determines the switching losses in power devices. It affects both hard-switching (at relatively lower switching frequencies, such as 100 kHz) and soft-switching (at higher switching frequencies, usually above 5-10 MHz) topologies.

2.1. Soft-Switching Output Capacitance Hysteresis Losses of Field-Effect Transistors

2.1.1. Sawyer-Tower Method

Here, we investigate the use of the Sawyer-Tower measurement technique as a powerful method to analyze the behavior of C_O, especially for soft-switching circuits [17]. Based on this method, we carried out a full study of C_O losses of Field-Effect Transistors [18].

Resonant-type power converters are an attractive solution to achieve large power densities at high frequencies due to their soft-switching behavior [19], [20]. Their applications include, among others, computer power supplies [21], radio-frequency (RF) power amplifiers in communication systems [22], [23], and wireless power transfer systems [24]. During a single switching cycle in these converters, the output capacitance, C_O, of the switching device is charged and discharged in a resonant manner dictated by the specificities of the topology, as a means of achieving soft-switching conditions. Since the device is in OFF state during the charging–discharging process of C_O, this ideally yields zero losses [17], [20].

However, it has been reported in recent research that, transition losses still exist due to dynamic charging and discharging of the power device's output capacitance under soft-switching conditions [20], [25]. The corresponding energy loss is attributed to a hysteresis loss [17], which is observed in large-signal charge versus voltage (QV) curves. Numerous works have reported such losses pertaining to different device structures: in Si Super- Junction (Si-SJ) transistors [26]; wide-bandgap (WBG) SiC transistors [27], and GaN high-electron-mobility transistors (HEMTs) [17], [20], [27]. The hysteresis energy loss in C_O is a function of the maximum (or peak) voltage, V_m, across the device's drain-source terminals, and is expressed as

$$E_{\text{diss}} = \int_0^{Q_1} v_{\text{ds}} dQ - \int_{Q_1}^{0} v_{\text{ds}} dQ$$

This energy loss adds an extra constraint on deciding the maximum voltage across a switching device for a given high- or very-high-frequency (HF or VHF) application. This is especially important in resonant converters where the device voltage stress could be quite high [23]. Prior knowledge of the dependence of hysteresis energy losses with V_m, for the available devices, would allow to select the most suitable operational voltage range for the circuit.

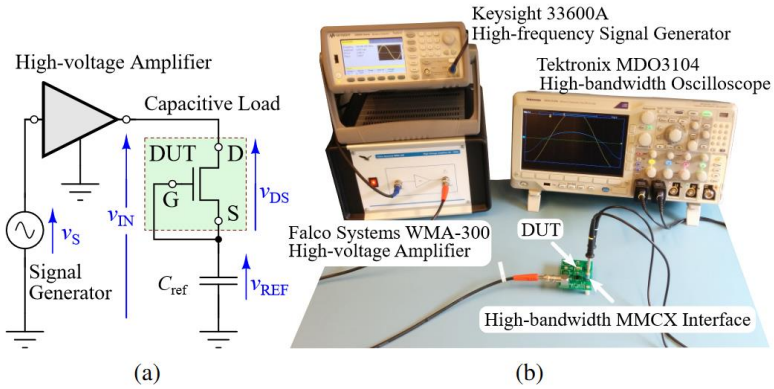

Fig. 3 (a) Schematic and (b) the experimental test setup of the Sawyer-Tower measurement technique used to analyze large-signal output capacitance.

In this section, four prominent field-effect transistor (FET) technologies were examined to observe their *QV* patterns. The study concerned soft-switching losses in the frequency range of 10 kHz to 1 MHz. The test circuit (see Fig. 3) operates such that the excitation voltage across the device drain-source terminals is of sinusoidal nature, while the gate-source terminals are shorted, i.e., $V_{GS} = 0$ V. High-voltage Si, Si-SJ, SiC and GaN devices are tested up to a V_m of 400 V. To make a comparative study, twelve FETs are selected, with a similar current rating of around 30 A. The part numbers, device technologies and other important details from the datasheets of the selected FETs are tabulated in Table 1.

Table 1: Commonly used Voltage Ranges in different Application areas.

DEVICES EVALUATED IN THE STUDY

Index	Technology	Voltage (V)	Part Number	Manufacturer	Current Rating (A) @ $T_C = 25\ ^\circ$C	$R_{DS(on)}$ (mΩ) typical	Package
Si-1	Si (planar)	500	SiHG32N50D	Vishay Siliconix	30	125	TO-247
Si-2	Si-SJ	650	NTHL110N65S3F	ON Semiconductor	30	98	TO-247
Si-3	Si-SJ	650	IPW65R110CFD	Infineon	31	99	TO-247
Si-4	Si-SJ	650	STW38N65M5	STMicroelectronics	30	73	TO-247
SiC-1	SiC	700	MSC090SMA070S	Microsemi	25	90	D3PAK
SiC-2	SiC	650	SCT3080AL	ROHM Semiconductor	30	80	TO-247
SiC-3	SiC	900	C3M0065090D	Cree	36	65	TO-247
SiC-4	SiC (cascode)	650	UF3C065080K3S	UnitedSiC	31	80	TO-247
GaN-1	GaN	650	GS66508T	GaN Systems	30	50	GaN*PX*
GaN-2	GaN	600	IGOT60R070D1	Infineon	31	55	PG-DSO-20-87
GaN-3	GaN	600	PGA26E07BA	Panasonic	31	56	DFN 8X8
GaN-4	GaN (cascode)	650	TPH3212PS	Transphorm	27	72	TO-220

QV patterns related to device output capacitances are experimentally obtained using the Sawyer-Tower technique, which relies on only two voltage measurements [17]. The circuit consists of a signal generator, a high-voltage amplifier, a fixed linear capacitor known as the reference capacitor, C_{ref}, and the device under test (DUT), as shown in Fig. 3. Since $v_{GS} = 0$ V, the DUT is essentially a capacitance equal to C_o for positive v_{DS} values [9]. The series combination of the DUT and C_{ref} is subjected to a large-signal input voltage v_{IN} created by amplifying a low-voltage signal v_S, having an excitation frequency of f. In steady state, a dc bias (V_{REF}) is built across C_{ref}; this renders v_{DS} to vary between 0 V and V_m [9]. Since the same current flows through C_o and C_{ref} in steady state, the ac voltage ($v_{ref} = v_{REF} - V_{REF}$) across C_{ref} is proportional to the variation of charge in both C_{ref} and C_o. Finally, the QV curves are extracted from the measured $\underline{v}_{REF}$ and $\underline{v}_{IN}$ data.

Fig. 4 plots experimental QV curves of the selected devices for $V_m = 400$ V and $f = 100$ kHz. The resulting E_{diss} is calculated by taking the area (shaded in orange in each sub figure) between the charging (solid red line) and discharging (solid blue line) paths. As the peak output voltage of the high-voltage amplifier was limited to ± 150 V (this limits V_m to 300 V), a HF transformer was utilized at the output of the amplifier to boost the voltage, so that $V_m = 400$ V was achievable. A C_{ref} of 1 nF was employed for all the devices, except for the Si devices 2 – 4, where a C_{ref} of 47 nF was used. This is because the large Q_o values ($\geqslant$ 250 nC) of these three devices cause too large a variation in v_{ref} for $C_{ref} = 1$ nF, and hence a drop in the available v_{DS} swing.

Fig. 4 shows that the DUTs exhibit diverse *QV* patterns, even within the same semiconductor types. In the Si family, the planar-Si structure shows negligible hysteresis while the SJ counterparts exhibit significant hysteresis with E_{diss} values greater than 1 μJ. The SJ devices show a distinct knee-type behavior in their discharging paths (indicated by a green circle), around where the region corresponding to E_{diss} is much larger, while the respective charging paths show much smoother transitions. The hysteretic area ceases around 200 V, beyond which the two paths coincide. SJ devices show much larger Q_o values (250 nC), while other devices—with comparable or lower values of on-state resistance, $R_{DS(on)}$— show much lower Q_o values (100 nC) at 400 V.

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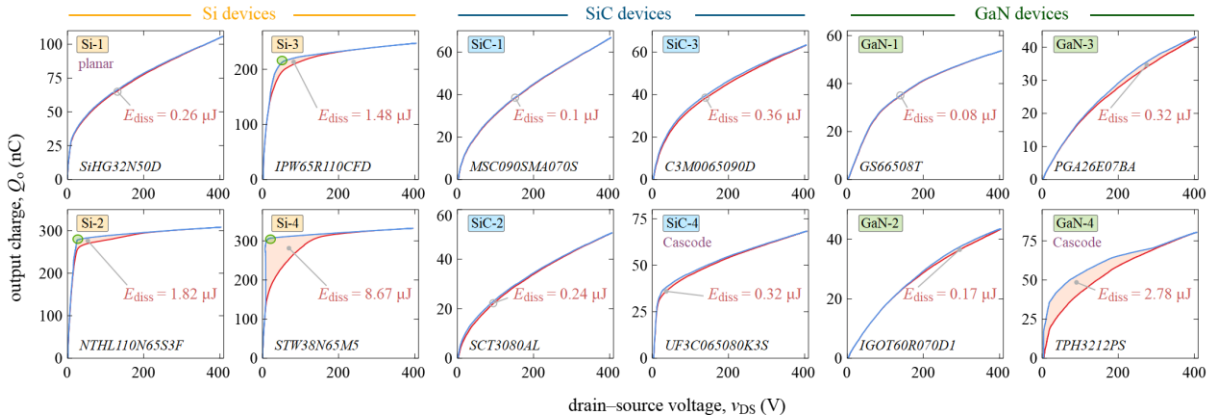


Fig. 4 Experimental QV (Q_O versus v_{ds}) curves of twelve different high-voltage transistors (current rating around 30 A): planar-Si device Si-1, Si-SJ devices Si-2 to Si-4, SiC devices SiC-1 to SiC-4 and GaN devices GaN-1 to GaN-4. The details of the devices are listed in Table 1. The solid red and blue lines correspond to charging and discharging paths, respectively; the hysteresis energy loss E_{diss} is indicated by the area between the two curves (shaded in orange).

The WBG devices SiC-1 and GaN-1 hardly show any hysteresis. The barely visible area between the charge–discharge curves of these two devices and the devices Si-1 and SiC-3, is symmetrically distributed within the whole v_{ds} range (i.e., the widening in the hysteretic area is symmetrical about V_m/2). An interesting observation is that the patterns of the cascode structures of the WBG devices (SiC-4 and GaN-4) deviate from their non-cascode counterparts, showing the knee-type behaviour characteristic of SJ structures. Furthermore, the cascode GaN device shows significant hysteresis compared to other GaN devices.

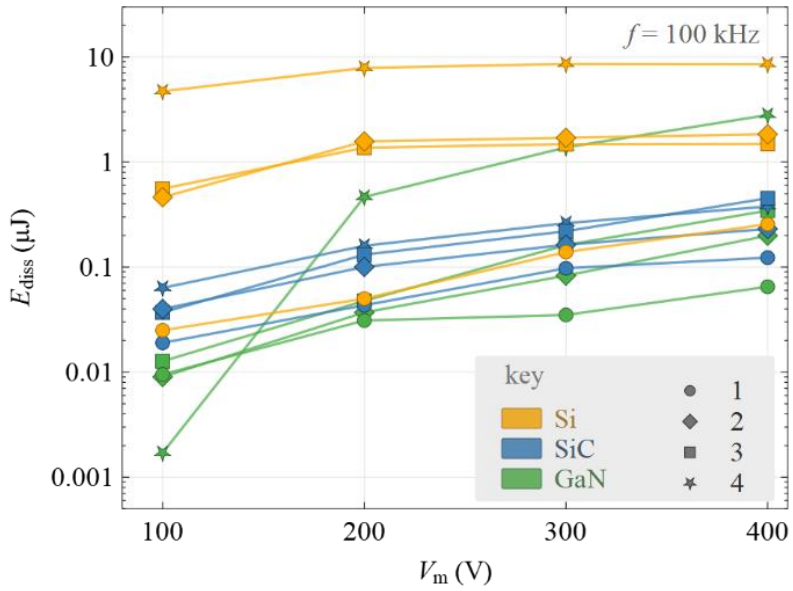


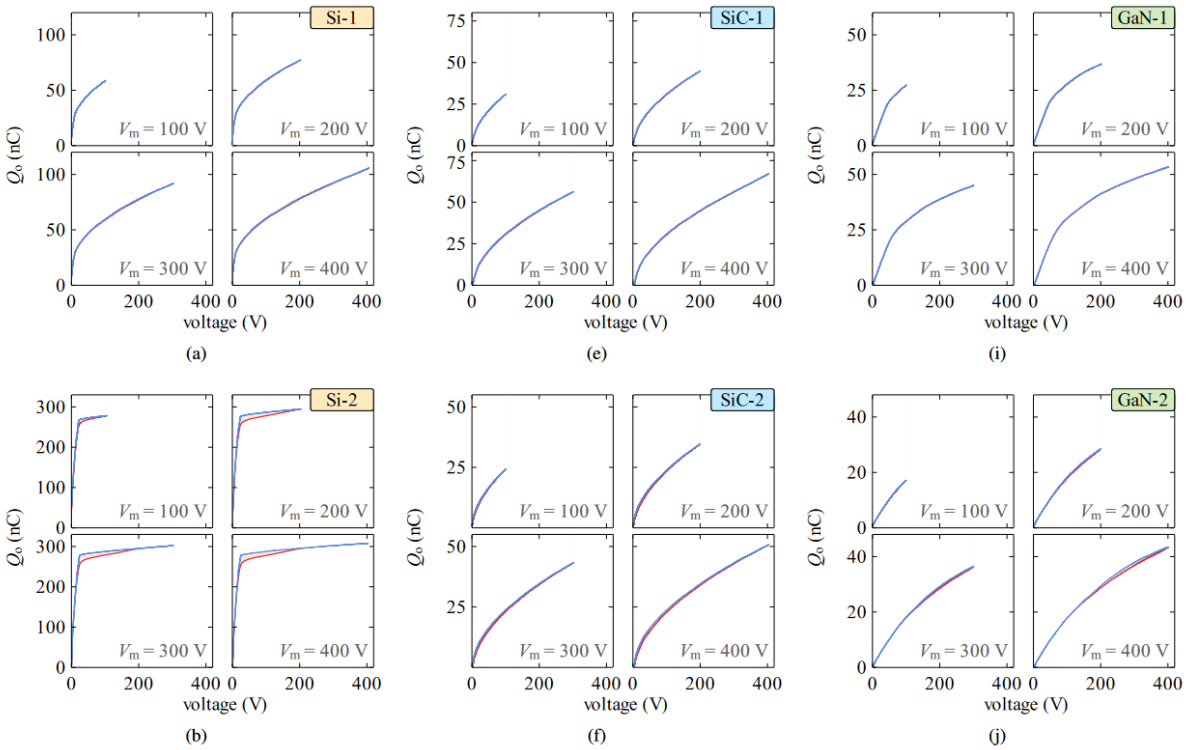
Fig. 5 Variation of E_{diss} with different V_m values for the twelve tested devices. V_m is varied between 100 and 400 V at 100 V steps.

Fig. 5 compares the variation E_{diss} with V_m for all the devices, while the excitation frequency is kept fixed at 100 kHz. Then, the QV patterns of each device is individually presented in Fig. 6 to explain their dependence on V_m. A clear observation is that the Si-SJ devices show a saturation of their E_{diss} values as V_m passes 200 V. This can be explained by observing Fig. 6(b) to (d). The hysteresis patterns exist even at 100 V and continue to grow up to 200 V. However, after 200 V, the charging and discharging paths coincide resulting in no hysteretic area. This suggests that the Si-SJ hysteresis is a low-voltage phenomenon, and that operation beyond, for example 200 V in the studied cases, do not result in additional

hysteresis energy losses. This could also be related to their significantly large C_o values (usually 10–100 nF) in the low v_{DS} range, which can be up to three orders-of-magnitude larger compared to the values at 400 V. The devices Si-1, SiC-1 and GaN-1, as expected from their 400-V results, exhibit no appreciable hysteresis even at low voltages—see Fig. 6(a), (e) and (i). Only a barely visible and symmetrically-spread hysteresis is present. However, Fig. 5 indicates that these devices show, although lower in value, an increasing E_{diss} with V_m.

The importance of the graphical observation of hysteresis patterns becomes apparent by looking into the GaN devices 1 to 3, which are from three different manufacturers. According to Fig. 5, the three devices (marked by circle, diamond and square symbols in green) show similar increasing-trends in their E_{diss} values with V_m. However, a major anomaly is observed in devices GaN-2 and GaN-3 when their QV patterns are looked into—see Fig. 6(j) and (k). The hysteresis area of the two devices widens in the high v_{DS} range (above 200 V), unlike in device GaN-1, which shows no such swelling. The hysteresis appears only for cases with V_m about 100 V, and the hysteresis pattern widens with increasing V_m. On the other hand, there is no visible hysteresis present at voltages below 100 V for these two devices (V_m values of 20 and 50 V were also tested and results showed no hysteresis); in this case, they act similar to device GaN-1, but in stark contrast to SJ devices, which clearly show a low-voltage hysteresis. This suggests that for these two GaN structures, Co hysteresis is a phenomenon that occurs only in the high v_{DS} range.

In addition, as Fig. 5 shows, device GaN-3 exhibits much larger E_{diss} values compared to device GaN-2, which is also verified by the relatively larger hysteresis patterns of the former. The superimposition of QV patterns corresponding to different V_m values on the same plot yields additional details between technology-specific differences in hysteresis losses. Fig. 7(a) shows that for device Si-3, the charge paths coincide for 100- and 400-V cases. However, for the cascode GaN device, as Fig. 7 (b) shows, neither the charging nor the discharging paths show any coincidence for the considered voltages (100, 200 and 400 V), suggesting a non-uniform dependence of the QV patterns with V_m. The device also shows a large increase of its E_{diss} value from 100 V to 200 V in Fig. 5. This is explained by its QV hysteresis patterns that appear to take place only if V_m is above 100 V, as Fig. 6 (l) indicates. Even above 200 V, the shapes of the hysteresis areas are quite different to other GaN devices. The shapes are more similar to that of Si-SJ devices.



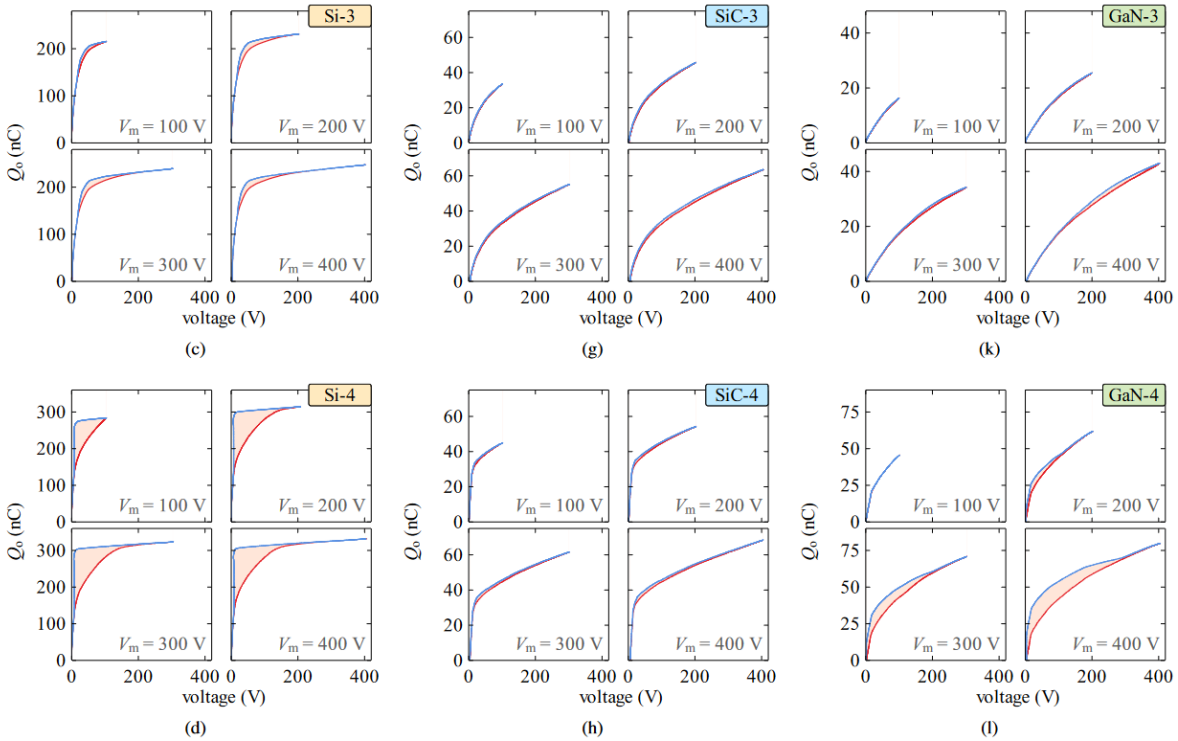


Fig. 6 Experimental results showing the variation of QV hysteresis patterns for various V_m values (at 100 kHz) for all the tested devices. The QV patterns exhibit diverse dependencies on V_m, among different devices and semiconductor technologies.

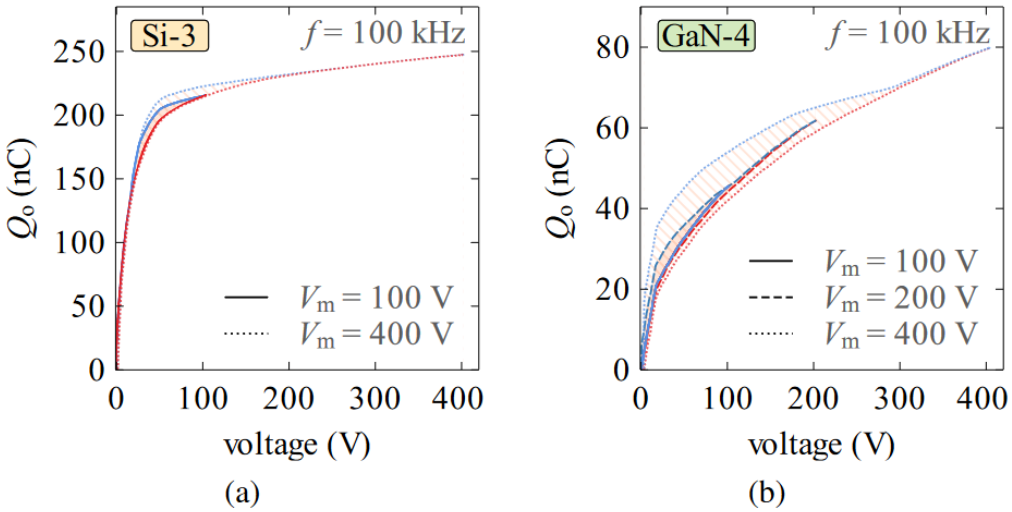


Fig. 7 Superimposition of QV hysteresis patterns of the devices (a) Si-3 and (b) GaN-4. The hysteresis pattern of device Si-3 at 400 V is a clear extension of the pattern at 100 V, with coincidental charging paths at each voltage. Device GaN-4 shows no hysteresis at 100 V; and at 200 and 400 V it shows hysteresis, but unlike device Si-3, it shows non-coincidental charging paths at each voltage.

2.1.2. Nonlinear Resonance Method

The need for high-amplitude sinusoidal voltage source in the ST method constrains the maximum voltage and frequency that can be applied to characterize large-signal C_o, and the typical values of dv/dt in switching transients, especially for GaN transistors, can only be achieved at very high frequencies, in the range of tens of megahertz.

Here, we proposed a large signal measurement method for C_O hysteresis losses based on the nonlinear resonance (NR) between the device output capacitance and a high-quality-factor inductor (Fig. 8) [31].

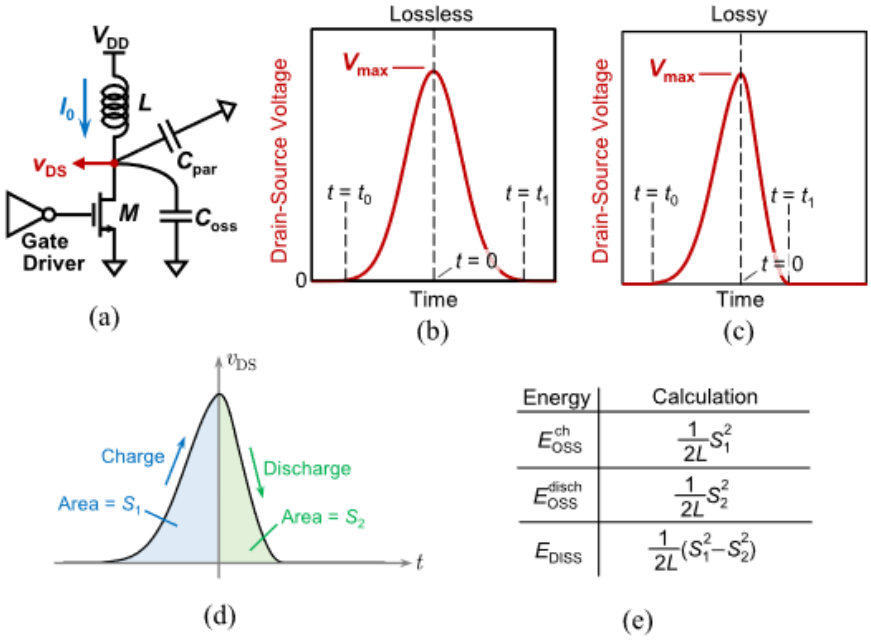


Fig. 8 Proposed method for large-signal C_O and E_{diss} measurement. (a) Circuit and samples of v_{ds} voltage waveforms for devices with (b) lossless and (c) lossy C_O charging/discharging processes. (d) Areas below v_{ds} waveform for charging (S_1) and discharging (S_2) processes translate to (e) C_O charging/discharging energies as well as the dissipated energy E_{diss}.

The inductor, charged in the on-state, resonates with the device output capacitance, when the DUT is turned off, charging and discharging its C_o. The deviation between the measured drain-source voltage waveform during the charging and discharging processes corresponds to losses dissipated during the soft-switching transient, which is calculated as

$$E_{\text{diss}} = \frac{1}{2L}(S_1^2 - S_2^2)$$

where S_1 and S_2 are the areas below the v_{ds} waveform during the charging and discharging process respectively [31].

Fig. 9 shows the measured and mirrored v_{ds} waveforms for a SiC device M1 and a Si superjunction (SJ) device M2. The measured resonant peak shows a symmetrical charging/discharging process, thus lossless behavior for the SiC device (Fig. 9a). A nonsymmetrical process for the Si SJ is observed (Fig. 9b), which corresponds to losses related to C_O charging/discharging.

The NR method is able to extract E_{diss} at high peak voltage (> 1000 V), high excitation frequency (> 40 MHz), and high dv/dt (> 120 V/ns). In addition, this method has a similar operation to actual resonant converters, which is not the case for the Sawyer-Tower method.

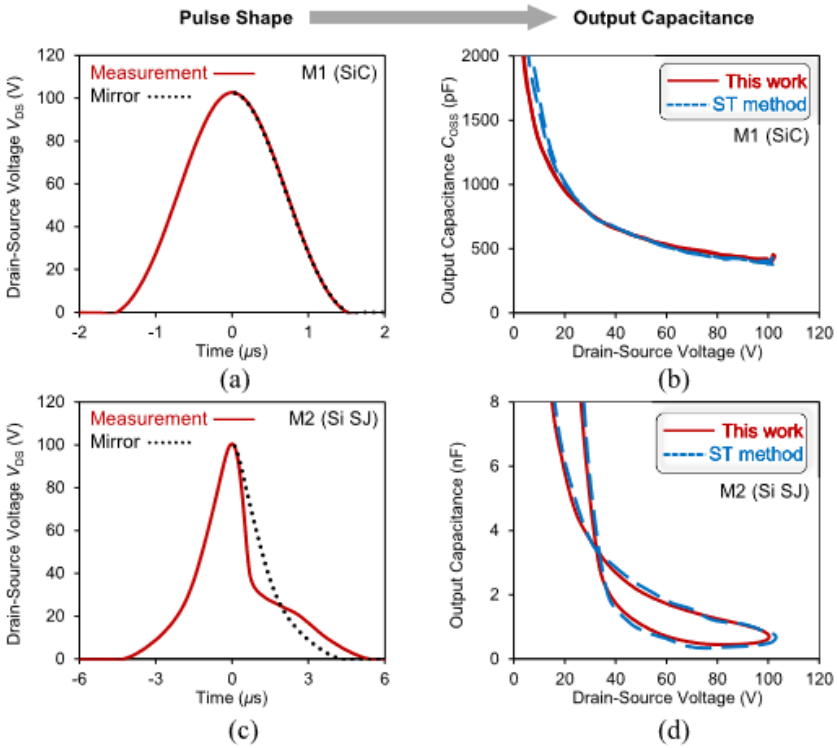


Fig. 9 (a) Measured v_{ds} (solid line) and mirrored waveform (dotted line) for M1. (b) Extracted C_O for M1 using the proposed method (solid line) and by ST method (dashed line). (c) Measured v_{ds} (solid line) and mirrored waveform (dotted line) for M2 shows a nonsymmetrical charging/discharging process. (d) Extracted C_O for M2 using the proposed method (solid line) and by ST method (dashed line).

2.1.3. Energy-based Nonlinear Resonance Method

Based on the nonlinear resonance between the device output capacitance and pre-calibrated inductor, we introduced an energy-oriented technique [32], in which the inductor current i_L is measured at the beginning and end of each pulse. E_{diss} is determined as the energy difference at the beginning ($E_0 = \frac{1}{2}LI_0^2$) and end ($E_1 = \frac{1}{2}LI_1^2$) of the resonance. The energy loss in the inductor is equal to $2\pi/Q$, where Q is the inductor quality factor and must be as large as possible. Thus, the dissipated energy is

$$E_{\text{diss}} = (1 - \frac{2\pi}{Q})(E_0 - E_1)$$

This method considers the DUT as a black box regardless of the device model in the OFF-state and only requires current measurements after carefully characterizing the inductor.

Fig. 10 shows the measurement results using the energy-based technique for a Si SJ device, where only 7.7 uJ of the initial inductor energy (17.3 uJ) has been recovered after the charging and discharging process.

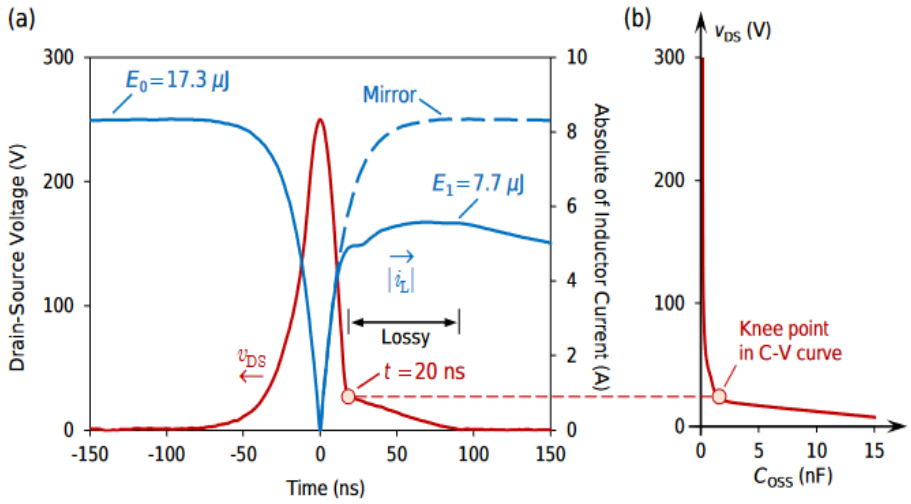


Fig. 10 Measured results for a Si SJ device from the energy-based method.

2.1.4. Implications on a Circuit Level: Calorimetric Method

Exclusive measurement of C_o-hysteresis loss in an actual resonant power converter is challenging. This is due to the requirement of small circuit-size in high-frequency operation that in turn creates measurement issues: for example, probing difficulties in electrical measurements and loss quantification issues in thermal/calorimetric methods [20] (due to thermal cross-coupling when several devices are involved).

Although an excellent technique [17], [18], [20], the Sawyer–Tower method cannot always replicate the actual v_{DS} waveform, and in some cases, the subsequent estimations could not fully explain the difference between measured versus predicted efficiencies in certain converters [20]. Thus, a direct and accurate method to measure hysteresis losses during actual circuit operation is required. On the other hand, existing calorimetric methods involve relatively slow systems that are also limited in accuracy, especially in mW-range power levels and they often determine system-level losses, and therefore, lack the ability to perform a complete loss break-down of a real converter in operation.

To emphasize the implication of C_o hysteresis losses on the circuit level, we proposed a calorimetric method [33] to measure the active device losses in a class-E inverter (Fig. 11). We demonstrate a complete and accurate loss breakdown of a class-E inverter operating at 10 MHz. A high-precision and compact flow-calorimeter is developed to accurately measure active-device losses at mW-level. This loss is then separated into transistor and gate-driving losses, using a combination of average current and voltage measurements. The transistor power loss is divided into ON-state (or the conduction loss, P_{con}) and OFF-state losses. A no-load concept is utilized to separate the gate-driving loss into gate loss and driver internal-loss. We have chosen the class-E topology, especially as a platform to measure the OFF-state loss of a transistor, as it offers several practical advantages:

1) The existence of only a single transistor eliminates the issue of thermal cross-coupling between two devices.
2) The path inductances between the input, the device branch, and the output can be incorporated into circuit inductances, thus permitting direct electrical measurements, without complicating the circuit operation.
3) All the parasitic shunt capacitances can be lumped together to a single shunt capacitance.

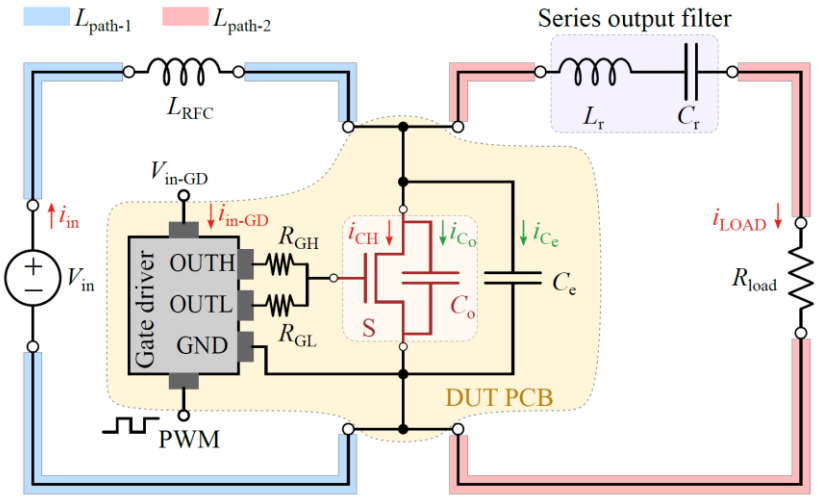


Fig. 11 Schematic of the class-E inverter.

In our analysis, we consider only field-effect transistors (FETs)—such as Si and SiC MOSFETS, and GaN HEMTs — as the switching device, which is denoted as S and undergoes zero-voltage-switching (ZVS). All the expressions and abbreviations for power refer to their average values, unless otherwise stated. The power losses generated in S and the gate driving sub-circuit constitute the active-device losses, P_{active}. The total power loss in a converter, $P_{loss\text{-}tot}$, consists of Pactive and passive-device losses, $P_{passive}$:

$$P_{loss\text{-}tot} = P_{active} + P_{passive}$$

The total input power, $P_{in\text{-}tot}$, of the converter is described as

$$P_{in\text{-}tot} = P_{loss\text{-}tot} + P_{load},$$

where P_{load} is the useful output power. In terms of average input power measurements, $P_{in\text{-}tot}$ can be expressed as the addition of the power-circuit input power (or the dc-link power), P_{in}, and gate-driver IC input power, $P_{in\text{-}GD}$:

$$P_{in\text{-}tot} = P_{in} + P_{in\text{-}GD}.$$

A FET model with its parasitic capacitances is shown in Fig. 12(a), highlighting the output capacitance. When the device is in ON state [Fig. 12(b)], a conduction loss, P_{con}, occurs which is a function of the ON-state resistance of the device channel, $R_{ch\,(v\text{drive})} = R_{DS(on)}$, and the channel current, i_{CH}. Here, V_{drive} is the voltage across the gate–source terminals of S, v_{GS}, in fully-ON state. In the class-E inverter, which is a load-resonant soft-switching converter, C_o gets charged and discharged during the OFF state [Fig. 12(c)] of the device. The corresponding v_{DS} waveform is shown in Fig. 12(d). This charge–discharge process of C_o results in a non-ideal hysteretic energy loss, E_{diss}, and can be calculated using a charge versus voltage (QV) curve as Fig. 12(e) indicates. The OFF-state losses related to the leakage current through the device channel are generally negligible, especially in comparison to E_{diss} losses for MHz-range frequencies [17]. Therefore, the total power loss is in S, at a switching frequency of f_{sw}, is given as follows, where $P_{diss} = f_{sw} \cdot E_{diss}$. Any loss related to gate driving is treated separately as shown next.

$$P_S = P_{con} + P_{diss}$$

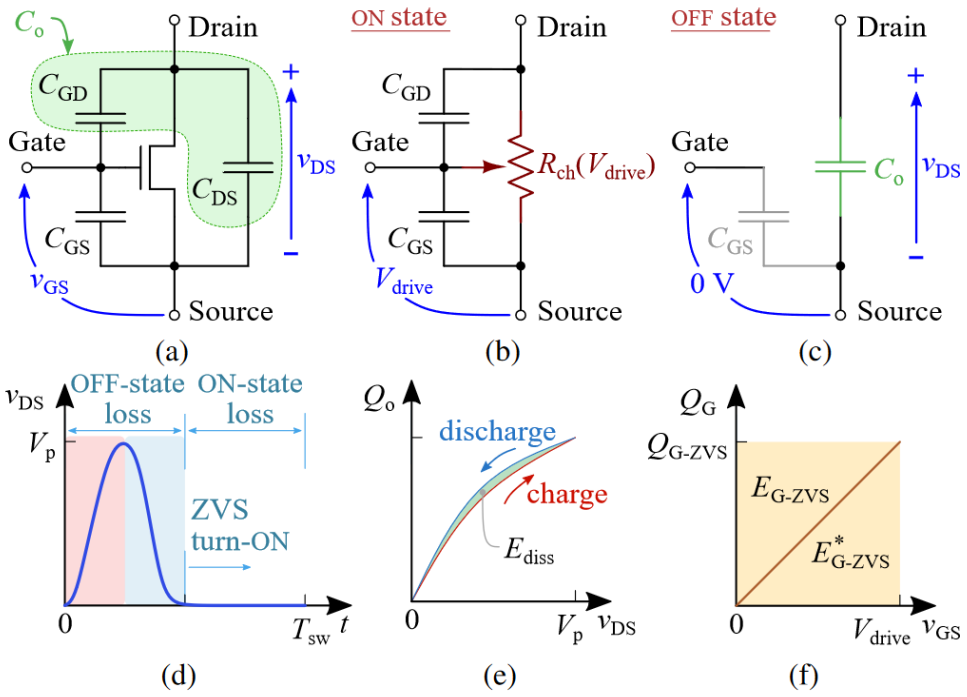


Fig. 12 (a) Model of a FET showing its parasitic capacitances, where $C_o = C_{GD} + C_{DS}$ is defined as the output capacitance. C_o is inactive during (b) the ON state of the device; and gets charged and discharged during (c) the OFF state of the device for a class-E inverter, where (d) the drain–source voltage, v_{DS}, shows a large-signal variation that generally occupies 50 % of the switching period, Tsw. (e) Related variation of the output charge (Q_o) with v_{DS} is represented by a QV curve; different charging (red line) and discharging (blue line) paths result in a hysteresis energy loss, Ediss, which is specified for a given maximum voltage V_p of v_{DS}. (f) Gate of the device gets charged up to $Q_{G\text{-}ZVS}$ during the turn-ON transient and then gets discharged at the device turn-OFF, resulting in a total gate-energy-loss $Q_{G\text{-}ZVS} \cdot V_{drive}$.

A typical gate-driver circuit consists of the gate-driver IC (denoted as GD) and external resistances R_{GH} and R_{GL}, as Fig. 13 illustrates. From the perspective of the power transistor, the traditional gate-driving is hard-gated, i.e., the gate-driving path is an RC circuit and involves no inductive components to achieve resonant gate-driving. For ZVS conditions, the total gate charge in S is denoted by $Q_{G\text{-}ZVS}$ as Fig. 12(f) shows. During the turn-ON transient of S, a power $P_{G\text{-}ON} = f_{sw} \cdot E^*_{G\text{-}ZVS}$ is dissipated in the resistances $R_{DS(on)\text{-}SH} + R_{GH} + R_{G\text{-}int}$ as marked by the area shaded in red in Fig. 13; and during the turn-OFF transient, a power $P_{G\text{-}OFF} = f_{sw} \cdot E_{G\text{-}ZVS}$ is dissipated in the resistances $R_{DS(on)\text{-}SL} + R_{GL} + R_{G\text{-}int}$ (area shaded in purple). Both these losses are independent of the resistance values and are determined by $Q_{G\text{-}ZVS}$, V_{drive} and f_{sw}. The complete gate loss (P_G) is therefore given as

$$P_G = P_{G\text{-}ON} + P_{G\text{-}OFF} = f_{sw}(E^*_{G\text{-}ZVS} + E_{G\text{-}ZVS}).$$

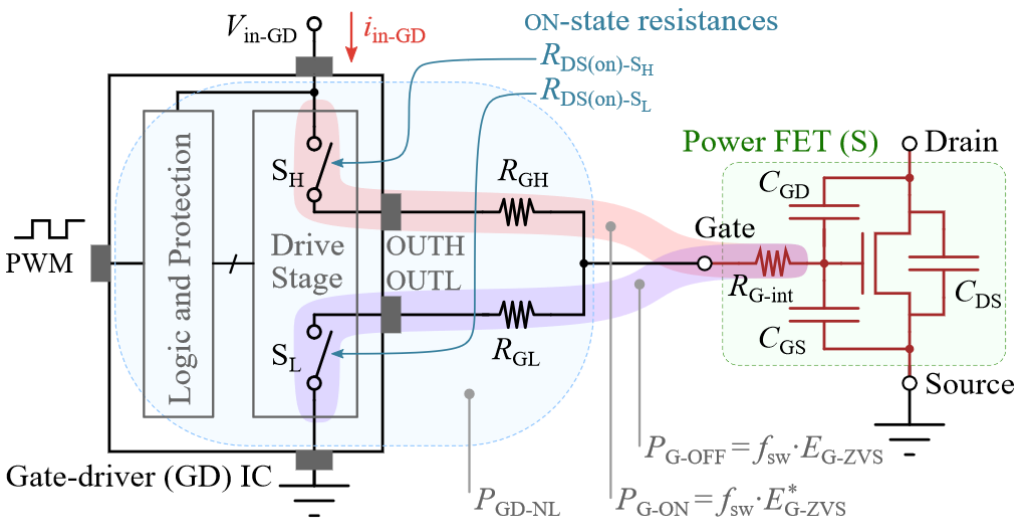


Fig. 13 An asymmetrical gate-driver IC has split outputs to control the turn-ON (through OUTH pin and R_{GH}) and turn-OFF (through OUTL pin and R_{GL}) processes of the power FET, S. In hard gating, the input power to the gatedriver IC, $P_{\text{in-GD}}$, is totally lost. This loss has two components: 1) losses inside the gate-driver IC, dominated by the switching losses of the drive-stage transistors SL and SH, and denoted as $P_{\text{GD-NL}}$; 2) a gate loss $P_{\text{G-ON}} + P_{\text{G-OFF}}$ in charging–discharging of the input capacitance of S.

There exists another loss (marked by the area shaded in light blue in Fig. 13 that is often overlooked in the gate-driving process, which is related to the drive stage of the IC; the two transistors SL and SH are hard switched and thus create their own output-capacitance-related losses and gate losses. It should be emphasized that this loss cannot be calculated from the power device characteristics as it is an attribute of the chosen gate-driver IC. In this work, we present a simple no-load method to measure this power loss, which is denoted here as $P_{\text{GD-NL}}$. Finally, the total power loss in gate driving is

$$P_{\text{in-GD}} = P_{\text{G}} + P_{\text{GD-NL}}.$$

A physical separation of the heat generated due to P_{active} and P_{passive} is possible. This is the underlying principle of the proposed measurement approach for the accurate breakdown of losses. The device under test (DUT) and the gate driver can be placed in a single PCB that is separated from the rest of the circuit. This requires longer connecting cables and the circuit should be tuned to achieve optimum operation. The use of calorimetric and electrical measurements, together with the approach for the full-breakdown of losses are discussed in the following subsections with reference to the block diagram of the measurement system depicted in Fig. 14.

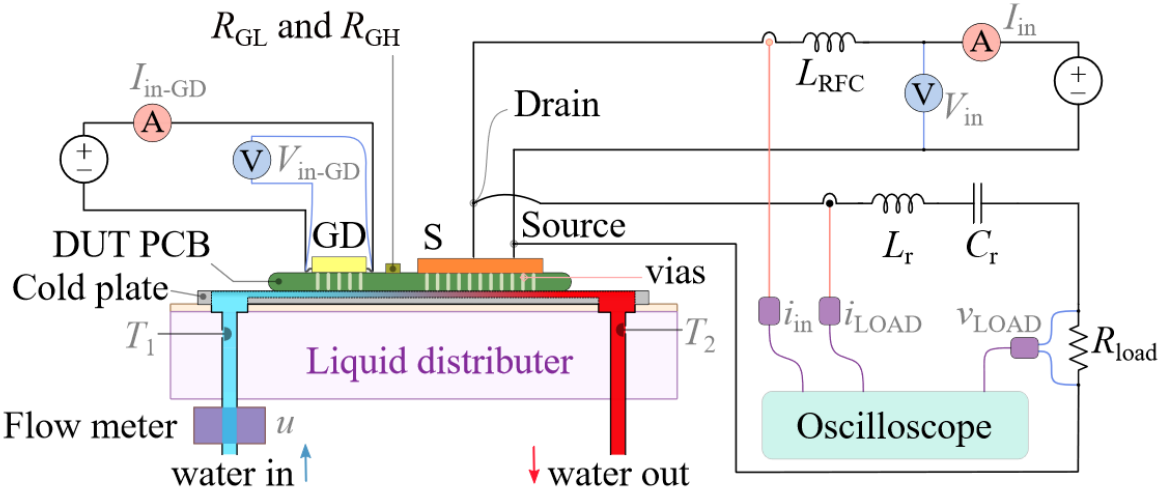


Fig. 14 Simplified block diagram of the presented measurement system showing the class-E inverter, the DUT PCB, and the application of calorimetric and electrical measurements. Two thermocouples (type K) measure the inlet and outlet temperatures, T_1 and T_2, respectively. An Elveflow MFS-A-5 flow meter accurately measures the flow rate u. I_{in}, V_{in}, $I_{in\text{-}GD}$ and $V_{in\text{-}GD}$ are average electrical measurements carried out with Fluke 87V DMMs. i_{in} and i_{LOAD} are total instantaneous current measurements carried out with Tektronix TCP0030A current probes and a MSO68B oscilloscope. v_{LOAD} is measured with a Tektronix THDP0200A differential voltage probe.

A novel and compact calorimetric unit (Fig. 15) was designed to evaluate the active-device losses in the circuit. The heat generated in the DUT and the gate driver are extracted by a microchannel-based cold plate fabricated on a piece of silicon (Fig. 15a), which is attached to the bottom of the PCB as Fig. 14 illustrates. A pressure controller is used to pass deionized water through the microchannels embedded in the cold plate. The cold plate is brought in to good thermal contact with the circuit using thermal grease, which enables a high level of heat extraction in a small form factor. This provides an additional benefit of cooling the active devices, permitting higher power dissipations without approaching critical temperatures. Due to its small size, the cold plate has a small heat capacity, resulting in short measurement times. The calorimeter evaluates the power dissipated on the PCB as

$$P_{calori} = \rho\, C_p\, u\, \Delta T.$$

Here, ρ is the density of the liquid with a specific heat of C_p; and u is the flow rate of the liquid. The temperature difference ($\Delta T = T_2 - T_1$) between the outlet and inlet water is measured using two thermocouples (Fig. 15b).

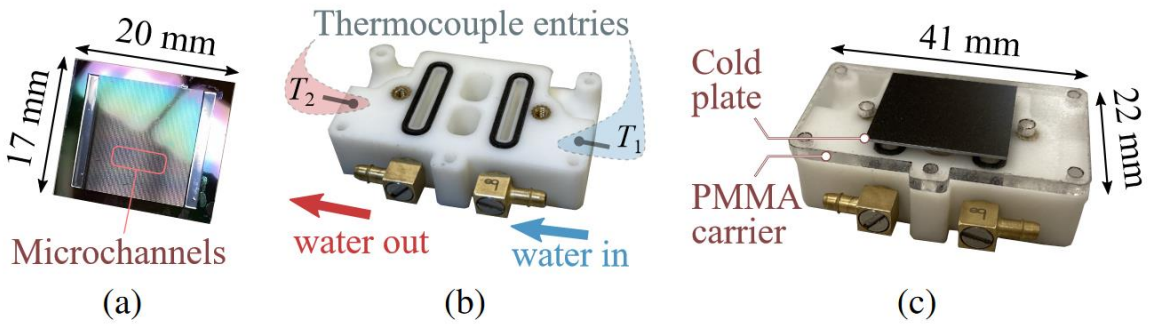


Fig. 15 (a) A silicon microchannel-based cold plate and (b) a 3d-printed liquid distributor, with entries for water and thermocouples, are assembled as (c) a compact calorimeter and an efficient cooler.

The accuracy of the calorimetric system was verified with a dc calibration as Fig. 16a shows. The power measured with the calorimeter approaches the value of the dc input power within a few minutes, where the error in measurement (Fig. 16b) is kept around 5 % for the whole power range, indicating very good accuracy. The system can measure a wide power range of 20 mW to 10 W; this is especially beneficial as E_{diss} vary quite significantly between different device structures and with f_{sw}.

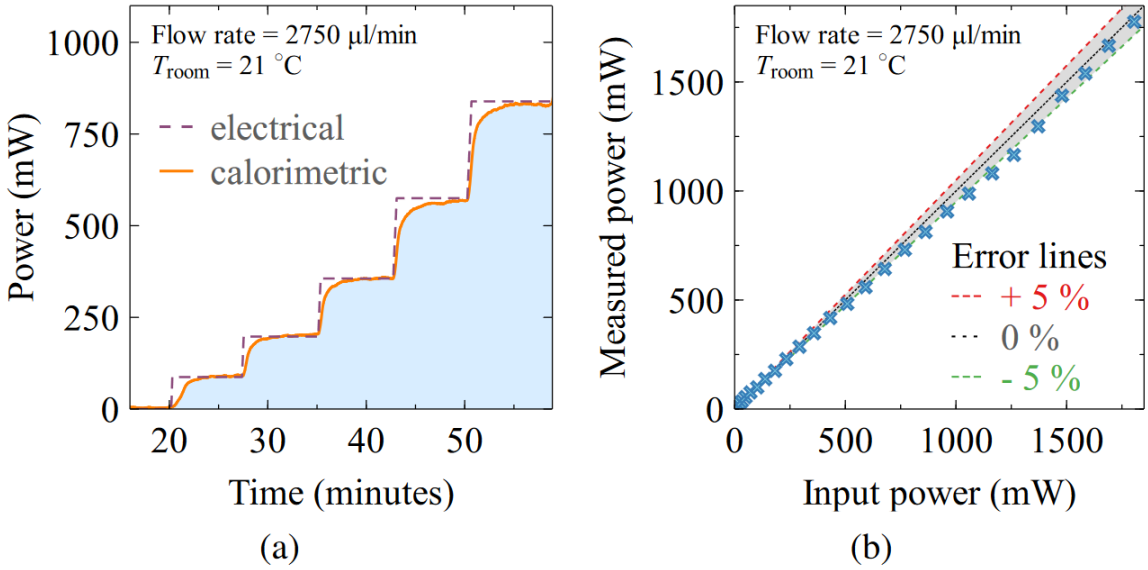


Fig. 16 (a) Example showing that the power loss measured with the developed calorimeter (solid line) approaches the dc input power $V_{DS} \cdot I_{DS}$ (dashed lines) quite fast, allowing 6–7 measurements within an hour at the given flow rate; the calorimeter tracks power levels as low as 100 mW with very good accuracy. Here, the transistor S is in ON state and a dc current I_{DS} was passed through it, while measuring the dc drain–source voltage V_{DS} (a 4-point measurement was used) (b) Calorimeter measurements exhibit good agreement with the dc input power, keeping the error ≈ 5 %.

The developed measurement concept is applied to identify individual loss components in a class-E inverter circuit operating at 10 MHz. A GaN Systems GS66504B GaN HEMT was used as the transistor and a Texas Instruments UCC27511A IC was used as the gate driver (details are listed in Table 2). The passive components were tabulated in

Table 3. The external shunt-capacitance C_e and series-filter capacitance C_r are multi-layer-ceramic (MLC) capacitors with a C0G (NP0) dielectric and have high quality-factors. The load resistance has a temperature coefficient of resistance (TCR) of 100 ppm/K, and thus, its variation within the operating temperatures here is negligible. The implementation of the circuit and the complete measurement system is shown in Fig. 17. An example of using the calorimeter to measure P_{active} is presented in Fig. 18: after the DUT board cools down from a preceding measurement, first the gate-driver circuit is turned ON and PWM is applied while V_{in} = 0 V; then V_{in} is gradually increased to the target operating mode. Once the thermal steady state is reached, P_{active} value is recorded. One major aim of this work is to evaluate E_{diss} as a function of V_p for a given transistor, which is achieved by varying the input voltage of the circuit. V_p values of 100 to 300 V, at 50 V steps, were considered. The ZVS conditions were maintained by changing the value of C_e for $V_p \geq 200$ V, while d = 0.5 was maintained. For $V_p \leq 200$ V, C_e was 0 and d was slightly adjusted from 0.5 to achieve ZVS conditions.

Table 2: List of active components.

LIST OF ACTIVE COMPONENTS

Component	Part No.	Specifications
Transistor (S)	GS66504B	650 V, 15 A, 100 mΩ
Gate driver (GD)	UCC27511A	Split output, 4.5–18 V, 4-A source, 8-A sink, SOT-23 (6) package

Table 3: List of passive components.

Component	Value	Unit	Remarks
R_{GH}	4.7	Ω	0402 package, 1/5 W, 1%
R_{GL}	1	Ω	0402 package, 1/5 W, 1%
R_{load}	25	Ω	Ohmite TGHMV25R0JE, ± 100 ppm/K, 0.23 °C/W, #187 tab terminals
L_{RFC}	10.8	μH	Air core, at 10 MHz, quality factor = 300
L_r	4.44	μH	Air core, at 10 MHz, quality factor = 343
C_r	56.9	pF	NP0 MLC capacitors, 1111 package
C_e	0–40.5	pF	NP0 MLC capacitors, 1111 package

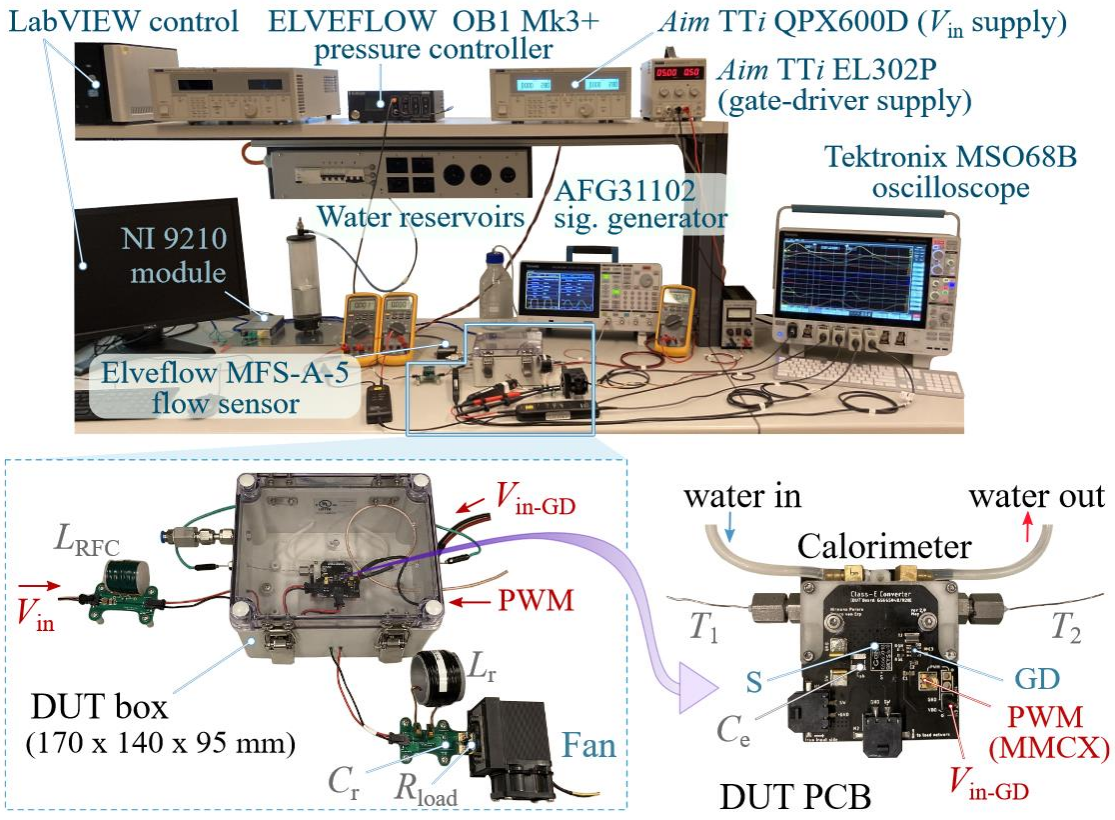


Fig. 17 Complete experimental system highlighting the measurement equipment and probes, calorimeter control system, class-E inverter circuit components, and the PCBs. The two active devices in the circuit (S and GD) and *C*e are built into a separate DUT PCB. A Tektronix AFG31102 signal generator is used to generate the PWM signals. For P_{active} measurement, a LabVIEWbased control system

is utilized: set the flow rate using a pressure controller, read the actual flow-rate using flow sensor; record the thermocouple readings T_1 and T_2; calculate P_{active} in real time.

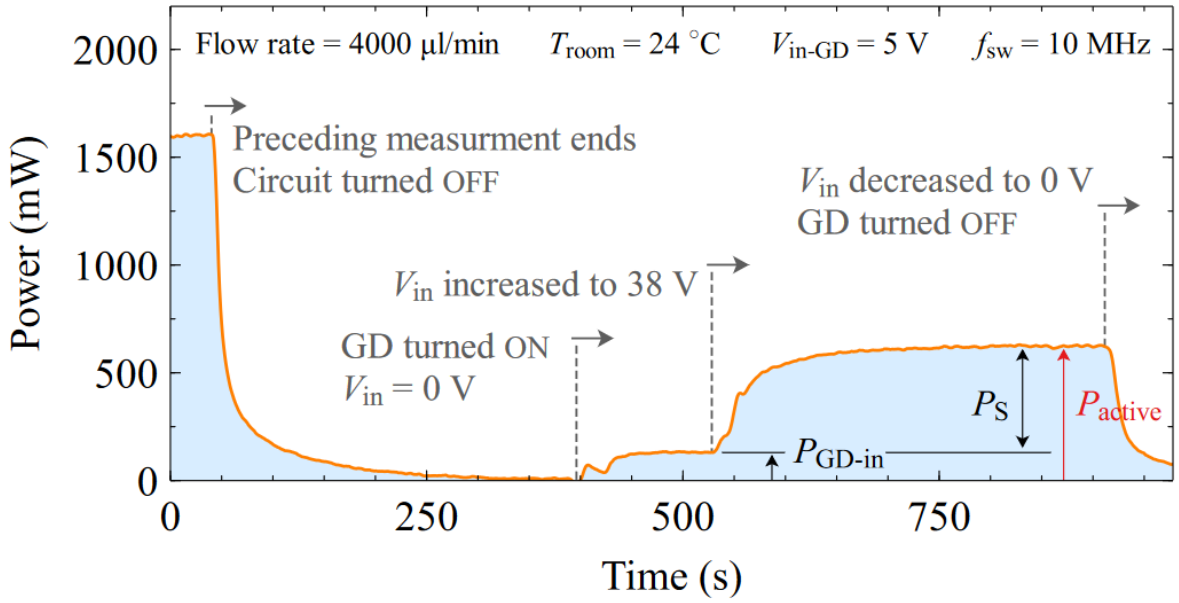


Fig. 18 Example showing the application of the developed calorimeter to measure P_{active} of the designed class-E inverter: the distinction between the gate-driving loss and the transistor losses is also observed.

Fig. 19(a) shows the total input power and the load power for different Vin values (at f_{sw} = 10 MHz). An input power of 102.6 W is reached for V_{in} = 81.4 V, which corresponds to a V_p of 300 V. Fig. 19(b) shows the breakdown of the corresponding power losses in the converter into passive device, transistor, and gate-driving losses. The passive-device losses are predominant and increase with the input power due to the increased average current in L_{RFC} and RMS current in L_r. The latter is responsible for the largest contribution as it is subjected to a large ac current, hence increasing its ac winding losses; on the other hand, L_{RFC} experiences a relatively small ac ripple as the input current is nearly dc in the topology.

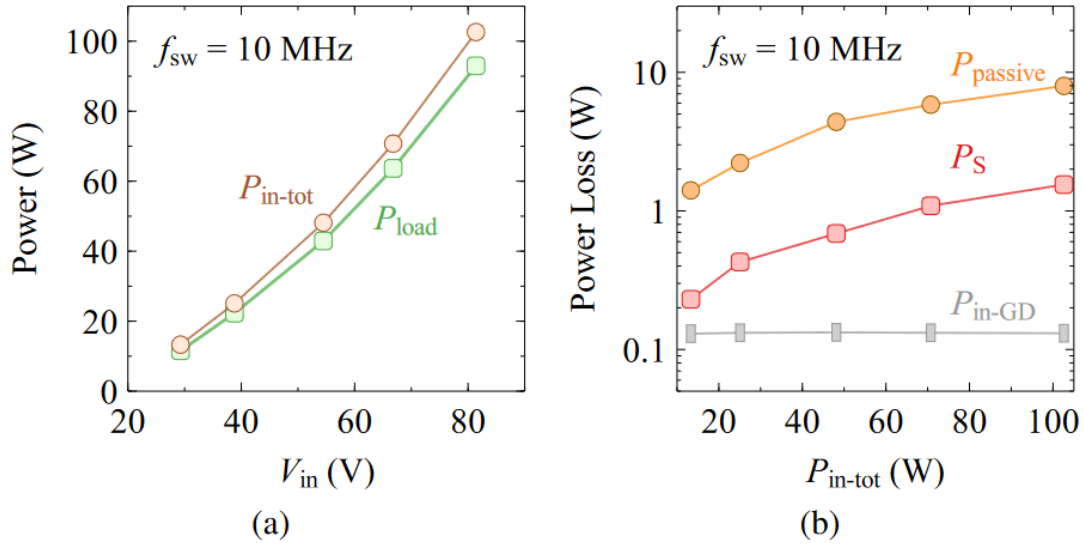


Fig. 19 Experimental results for the designed class-E inverter operating at f = 10 MHz. (a) Variation of the total input power, P_{in-tot}, and the load power, P_{load}, with input voltage. (b) Breakdown of the losses with P_{in-tot}: the gate-driving loss P_{in-GD}, transistor loss P_S and passive device losses $P_{passive}$. The presented method is capable of measuring mW-range power levels, enabling accurate loss and efficiency calculations.

Referring to Fig. 19(b), it is observed that the losses in the transistor also increase with $P_{\text{in-tot}}$. This is due to two reasons. On the one hand, the conduction loss increases with V_{in} (or $P_{\text{in-tot}}$) because of the increased RMS current through S—note that $R_{\text{DS-on}}$ of S does not vary significantly (stays around 100 mΩ) for the considered power-dissipation range. On the other hand, the OFF-state loss increases with V_{in}, or more specifically with V_{p}, due to the hysteresis loss that occurs in C_{o} while it is being charged and discharged during the OFF-state in each cycle.

Fig. 20 plots the corresponding Ediss values, where $R_{\text{DS(on)}}$ in is multiplied by a positive factor k_{dyn} to evaluate P_{con}. The corresponding Sawyer–Tower results, reported by Zulauf et al. [20], are also marked (in solid blue). The comparison reveals that, as the value of k_{dyn} increases, the measured E_{diss} value deviates from the Sawyer-Tower results, suggesting that dynamic $R_{\text{DS(on)}}$ degradation is small in class-E circuit. This could be explained by the short duration of the peak OFF-state-voltage in class-E circuit, which can create different charging dynamics during the OFF state; however more studies are needed to understand such effects.

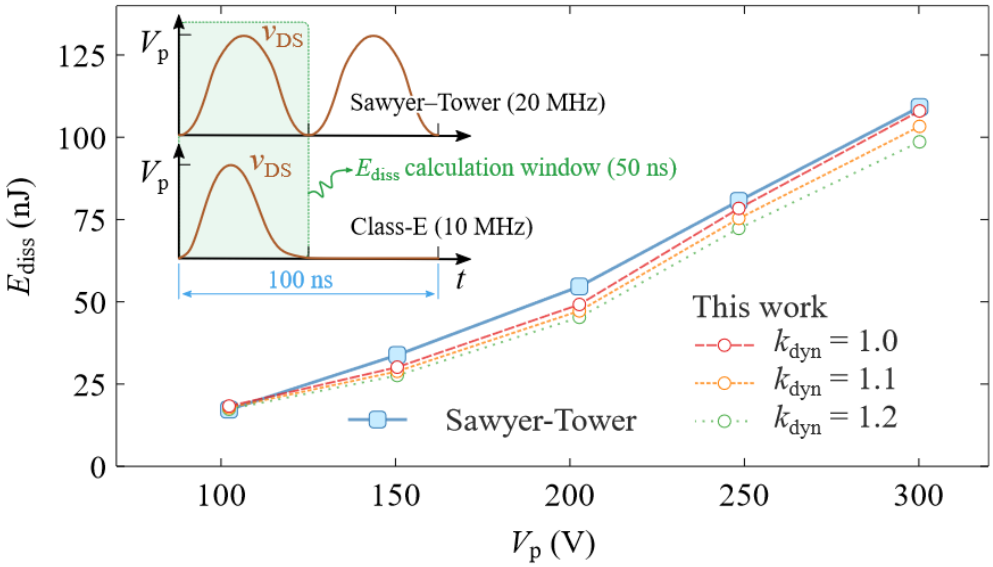


Fig. 20 Variation of output-capacitance hysteresis losses with V_{p} for the GS66504B transistor in actual converter operation at 10 MHz. k_{dyn} = 1.0, 1.1 and 1.2 correspond to 0, 10, and 20 % increase in the $R_{\text{DS(on)}}$ value (measured in dc conditions) to investigate dynamic $R_{\text{DS(on)}}$ effects. The corresponding Sawyer–Tower results are marked in solid blue (from Zulauf et al. [20]). Note that the v_{DS} waveform of a class-E inverter at 10 MHz with d = 0.5 has a 50 ns of charge–discharge time for C_{o}; this corresponds to a Sawyer–Tower excitation at 20 MHz.

Note that although the circuit operates at f_{sw} of 10 MHz (T_{sw} = 100 ns), the actual charging–discharging event of C_{o} corresponds to a duration of 50 ns (for d = 0.5), or an effective frequency of 20 MHz (see Fig. 20). Therefore, the Sawyer–Tower results at 20 MHz should be used for comparison to get a similar charge–discharge frequency, as most GaN devices show a frequency dependence for E_{diss}. In addition, C_{e} is subjected to the same voltage swing as C_{o}. Since C_{e} was chosen to have a low equivalent-series-resistance (ESR), any ESR losses can be assumed negligible for the considered RMS current through the device branch; this assumption was validated by the observation of insignificant temperature rise in C_{e} during the circuit operation for all power levels.

Fig. 21 breaks down the active-device losses at f_{sw} = 10 MHz into the four main components for the case of V_{in} = 81.4 V (or equivalently V_{p} = 300 V). The results reveal that P_{diss} dominates active-device losses with a contribution of 64.28 %, which amounts to 1.08 W. This observation demonstrates the major implication of output-capacitance hysteresis losses in MHz-range operation, inhibiting the ideal

advantages of zero switching-losses (or OFF-state losses) offered by soft-switching operation. It is also important to note that the gate-driving losses in total amount to 7.82 % of P_{active}, which is not negligible.

This comprehensive breakdown of active-device losses aids the power electronic circuit designer to identify the causes for losses and choose the best transistor and gate-driver IC combination for the most favourable design. The measurement approach can be extended to other resonant converter circuits, but the complexity depends on the topology. A single gate-driver can be used by employing a bootstrap method for direct $P_{\text{in-GD}}$ measurement. And dead-time should not extend much beyond the required minimum value to avoid errors in conduction loss calculations.

In conclusion, we have demonstrated a complete loss-breakdown concept for a class-E inverter. The presented ideas allow to compare and separate the active-device losses into transistor ON- and OFF-state losses, as well as gate and internal-gate-driver losses. An experimental method with mW-level precision is presented and utilized to measure these losses at 10 MHz. The approach provides an accurate and in-converter evaluation of the hysteresis losses related to the output-capacitance of transistors. It was shown that the distinction between transistor-related gate loss and the driver-related internal loss is important for the loss characterization of MHz-range converters.

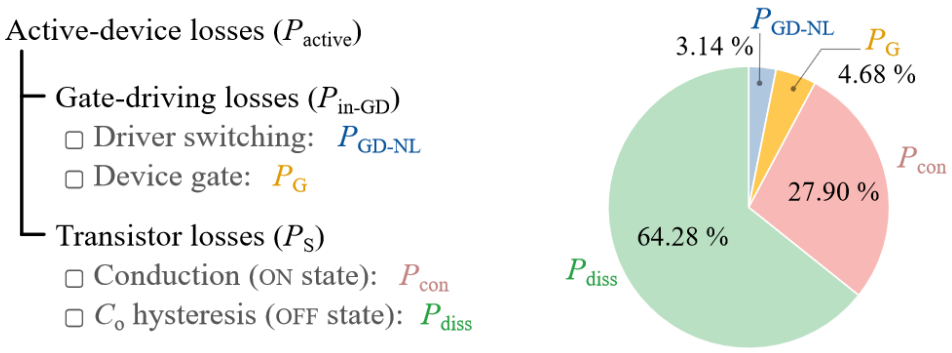


Fig. 21 Complete breakdown of the active-device average power losses in the tested class-E inverter at 10 MHz. Here, total active-device loss P_{active} = 1.68 W, total input power $P_{\text{in-tot}}$ = 102.6 W and V_{in} = 81.4 V. S is a GS66504B GaN HEMT and GD is a Texas instrument UCC27511A IC. C_{O}-hysteresis loss is the major contributor accounting for 64.28 % of losses. These results are based on in-circuit measurements (without using any estimation based on indirect measurements) and therefore represent actual operating losses.

2.2. Hard Switching Losses of in Power FETs

High-frequency (HF) power converters play an important role in high-power-density applications. For soft switching circuits operating in such frequencies, large-signal hysteresis losses caused by the output capacitance of certain field-effect transistors (FETs) can be a major hindrance as we discussed in previous sections. In 30-A devices for example, these losses vary from a few tens of nanojoules to a few microjoules at 400-V operation, for frequencies below 1 MHz [18]. In contrast, hard-switching energy losses, dominated by the turn-on loss, are typically around 50–500 μJ at 400 V for the same devices. But more importantly, in hard-switching converters, the role of C_{o} is fundamentally different as opposed to in soft-switching operation. Therefore, the effects of any large-signal anomaly in C_{o} for hard-switching operation—for instance, a change in output charge—first need to be understood from a topological perspective.

In this section, we introduce an energy-based method to capture and isolate the losses related to output capacitance in hard-switching circuits. Based on the proposed concepts, an experimental technique relying on average electrical measurements is developed to obtain the output-charge versus voltage (QV) curve for a given FET, which is true to the charge capacity of C_{o} in actual hard switching. The technique

can create different switching speeds and is independent of deadtime, switching frequency and device on-resistance, making it a potent tool to characterize QV behavior and C_o losses.

In hard-switching applications, the energy losses related to the output capacitance reflect the minimum switching energy and are load-independent. Conventional hard-switching tests cannot fully set apart the C_O-related hard-switching losses, and small-signal-based charge-voltage (QV) curves may fail to represent such large-signal losses.

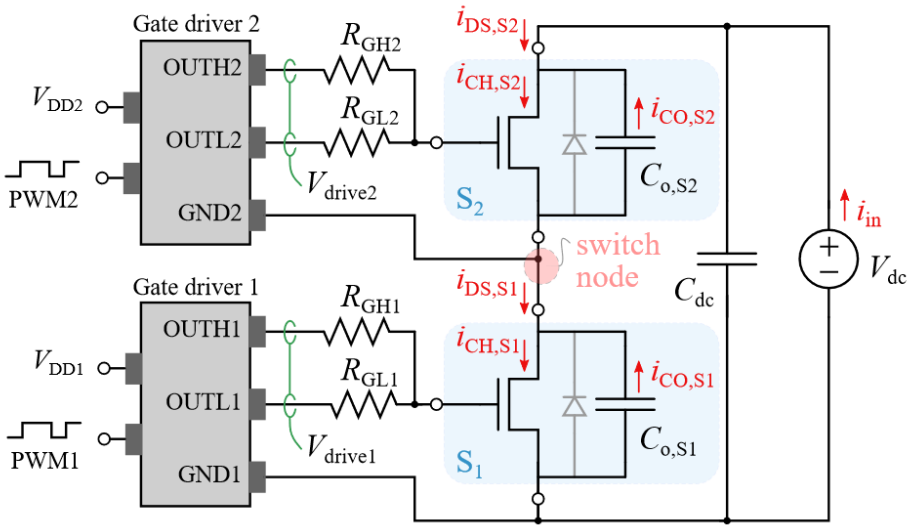


Fig. 22 No-load topology consists of a half-bridge circuit where the bottom and top devices (S_1 and S_2) are switched complementarily with asymmetrical gate driving. A dc-link capacitance C_{dc} is placed very close to the switching devices. C_O of each device is represented as a capacitance in parallel with drain–source terminals. Any third-quadrant operation (denoted by the diodes) is inhibited due to the non-existence of any load current at the switch-node.

We developed a measurement technique to obtain the QV curves of power devices subjected to actual hard switching by using a half-bridge no-load circuit [35], as shown in Fig. 14. The switch node is left floating, involving zero load current. The channel, drain, and output-capacitance currents are also shown. The circuit features an asymmetrical gate-driving scheme. The operation of the circuit can be analyzed through six operating modes as Fig. 23 illustrates, where important waveforms during switching transitions are given in Fig. 24. Throughout this work, the following is maintained for the external gate-driver resistor values: R_{GH1} = R_{GH2} and is denoted by the general term R_{GH}; R_{GL1} = R_{GL2} and is denoted by the general term R_{GL}.

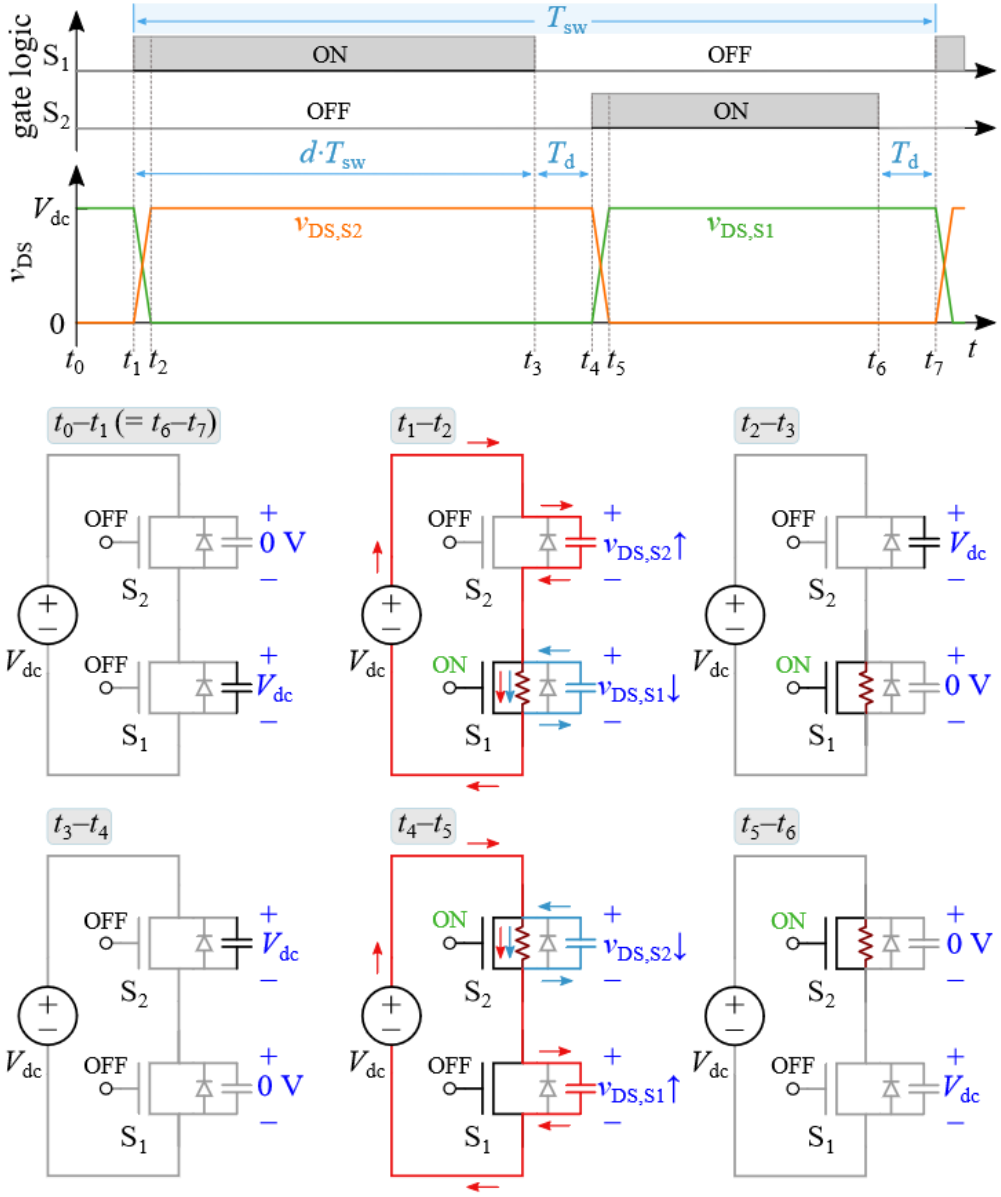


Fig. 23 Operation of the no-load circuit can be divided into six modes, where $T_{sw} = 1/f_{sw}$ is the switching period, T_d is the dead-time, and d is the duty ratio. During the dead-times (t_0–t_1 and t_3–t_4), as well as during the on-periods (t_2–t_3 for S_1 and t_5–t_6 for S_2), no charge or discharge process related to output capacitances occurs; such a process would only take place during switching transitions. During t_1–t_2, $C_{o,S1}$ gets discharged while $C_{o,S2}$ gets charged; during t_4–t5, $C_{o,S1}$ gets charged while $C_{o,S2}$ gets discharged. The fixed voltage source V_{dc} acts as the energy source for the two charging processes.

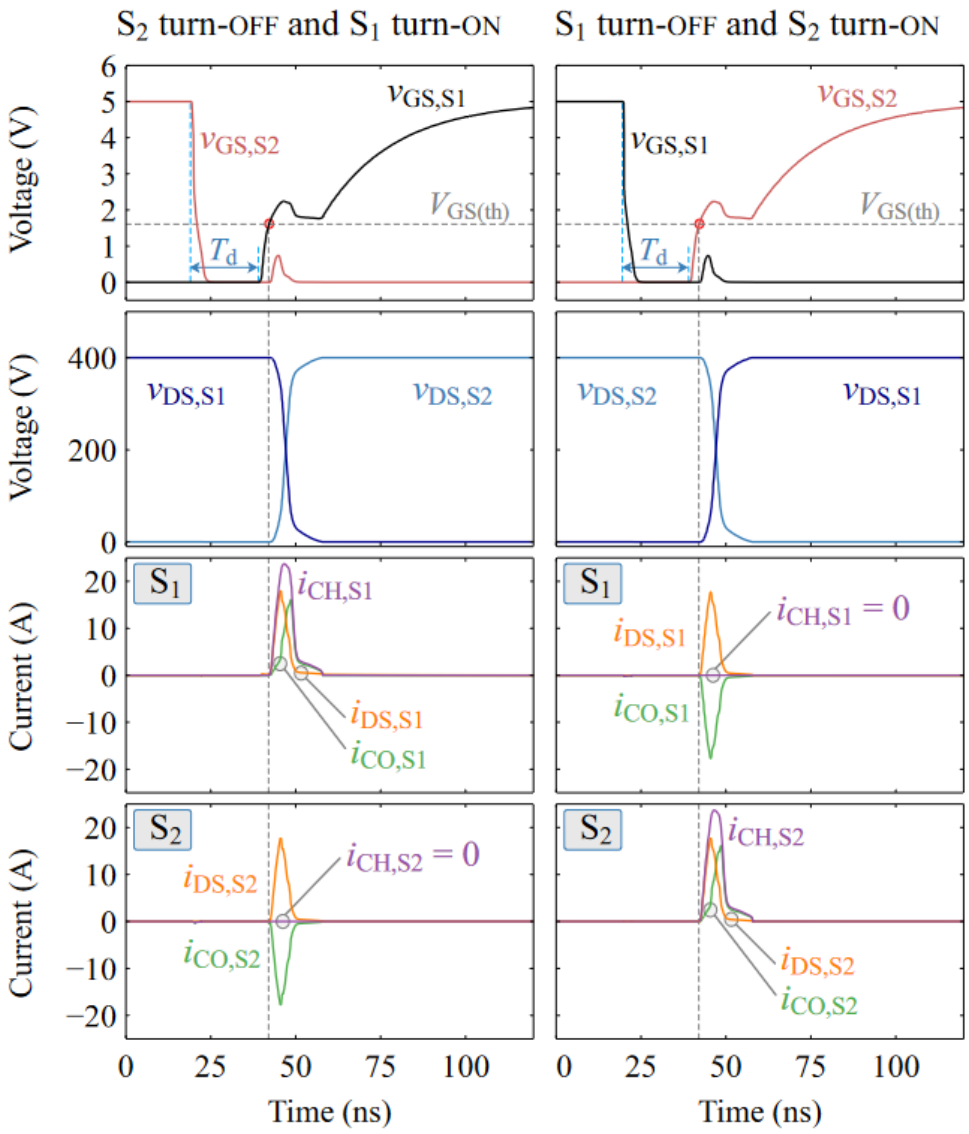


Fig. 24 LTspice simulation results showing the turn-on and turn-off transitions of S_1 and S_2 in the no-load circuit, where V_{dc} = 400 V, f_{sw} = 100 kHz, d = 0.5, T_d = 20 ns, R_{GH} = 20 Ω and R_{GL} = 0.1 Ω. During the dead-times, the voltages $v_{DS,S1}$ and $v_{DS,S2}$ stay at their before-dead-time values as there is no load current to charge or discharge the switch-node capacitance. When a device turns on, it experiences a channel current larger than its drain current due the discharge of its output capacitance; the already-off device experiences zero current in its channel.

During the turn-on transition of S_1 (t_1–t_2 in Fig. 23), no current commutations take place as there is zero load current. Therefore, as soon as v_{GS} approaches $V_{GS(th)}$, the voltage commutation commences, unlike in a DPT circuit. Since the channel of S_1 is now conducting (although not fully enhanced), its output capacitance $C_{o,S1}$ discharges through its own channel, adding a current component $i_{CO,S1}$ to the channel. While this self-discharge happens in S_1, the output capacitance of S_2, $C_{o,S2}$, gets charged by the dc voltage source; this causes an additional second current component to pass through the channel of S_1 such that $i_{CH,S1} = i_{CO,S1} + (-i_{CO,S2})$ (see Fig. 24). For this charging process of $C_{o,S2}$, the channel of S_1 acts as a resistance (variable in nature) in series with the dc voltage source; thus, this loss is independent of the value or nature of R_{ch}. At the end of the voltage commutation period, two loss components are identified in the channel of S_1, which are caused solely due to device capacitances. The first is the discharge loss of $C_{o,S1}$ that is equal to the energy that was stored in $C_{o,S1}$ at off-state (equal to $E_{o,S1}$). The second is the loss incurred due to the charging of the output capacitance of the complementary device ($C_{o,S2}$) that is equal

to the co-energy of $C_{o,S2}$, $E^*_{o,S2}$. Thus, the total energy loss in S_1 at its turn-on transition in the no-load circuit—due to the charging and discharging of device output capacitances—is equal to

$$E_{\text{on-Co(NL)}} = E_{o,S1} + E^*_{o,S2}.$$

And for the case where $S_1 = S_2$, which is the typical case in half-bridge configurations, we get

$$E_{\text{on-Co(NL)}} = E_o + E^*_o = Q_o V_{dc}.$$

The same analysis can be carried out for the turn-on transition of S_2 (t_4–t_5 in Fig. 23). As Fig. 23 illustrates, all the other operating modes in the circuit are inactive modes that do not involve any charge–discharge processes of C_o, and therefore assume no change in v_{DS}, as Fig. 24 also shows. Thus, the total energy

$$E_{in(NL)} = 2\, Q_o V_{dc}$$

drawn from the dc voltage source in each switching cycle is completely dissipated as heat. It is important to note that during practical operation, C_{dc} acts as the dc voltage source that supplies the energy ($E_{\text{on-Co(NL)}}$) required for a single switching transition. C_{dc} then gets charged by the external voltage source before the next switching transition takes place; this process however involves negligible energy loss. This is because as C_{dc} is very large, the voltage drop caused by the extraction of an amount of charge equal to Q_o is insignificant. The above analysis shows that the input energy in the no-load circuit is independent of 1) the time variations of R_{ch} and its on-state value $R_{DS(on)}$; 2) deadtime and duty cycle, as energy-transfers take place only during voltage-commutation periods; and 3) switching frequency, as long as Q_o does not show any frequency dependence. Moreover, $E_{in(NL)}$ is not affected by any C_o-hysteresis as it is determined by the final Q_o value.

The developed QV measurement method is based on the measurement average electrical input power P_{in}. The input energy E_{in} is then calculated by P_{in}/f_{sw}. For the case where $S_1 = S_2$, we obtain that

$$P_{in} = E_{in} \cdot f_{sw} = 2\, Q_o V_{dc} \cdot f_{sw},$$

and the hard-switching QV curves can be obtained by sweeping V_{dc} and calculating the corresponding Q_O as

$$Q_o = \frac{1}{2}\frac{P_{in}}{V_{dc} f_{sw}}$$

where P_{in} is the average total input power measured with high-precision multimeters and f_{sw} is the switching frequency.

Fig. 25 shows the experimental system with measurement equipment, the control unit and one of the no-load circuits. A MAGNA Power TSD800-18/380 power supply was used to supply dc-link voltages up to 400 V. The dc-link capacitance was 2.2 μF. The average input current I_{in} and voltage are measured using Fluke 87V digital multimeters (DMMs).

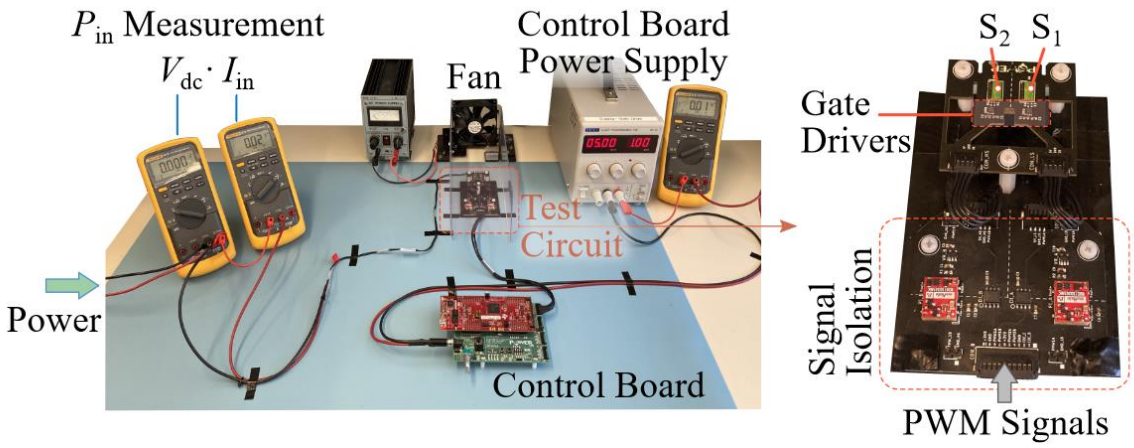


Fig. 25 Experimental test system with electrical measurements. The gate driver supply voltages and the PWM signals were isolated using two dc-dc converters and digital-signal-isolators.

The developed measurement method was applied to compare GaN, SiC, Si devices with similar voltage and current ratings (Table 4), and the obtained QV curves are shown in Fig. 26 to Fig. 28, respectively. The datasheet-based curves (marked by solid black lines) were obtained by integrating C_{oss} with v_{DS}. The Sawyer–Tower measurements (marked by red and blue dashed lines for charge and discharge processes) were performed at an excitation frequency of 100 kHz and a peak voltage (V_p) of 400 V.

Table 4 Devices Evaluated for Hard Switching Losses

Label	Part Number	Voltage (V)	Current Rating (A) @ T_C = 25 °C
GaN-1	TPH3212PS	650	27
GaN-2	GS66508T	650	30
SiC-1	MSC060SMA070B	700	39
SiC-2	C3M0065090D	900	36
Si-1	STW38N65M5	650	30
Si-2	NTHL110N65S3F	650	30

The hard-switching results for the two GaN devices closely follow the datasheet values (with a maximum deviation of 9 % for device GaN-2 at 100 < V_{dc} < 200 V). The Sawyer-Tower curves also exhibit good agreement up to 300 V but tend to deviate moderately beyond that. Sawyer-Tower results for device GaN-1 from a previous work have shown that the hysteresis pattern emerges suddenly after V_p > 100–150 V [18], when different V_p values were tested; in Fig. 26a, the hard-switching curves do not show any abrupt deviation in their trends above 100 V, affirming that $E_{in(NL)}$ depends only on the final Q_o value and that C_o-hysteresis has no effect on it. The tests were repeated using different samples of the devices and the results (marked by additional circles on the two plots in Fig. 26) further confirm the validity of the measurements.

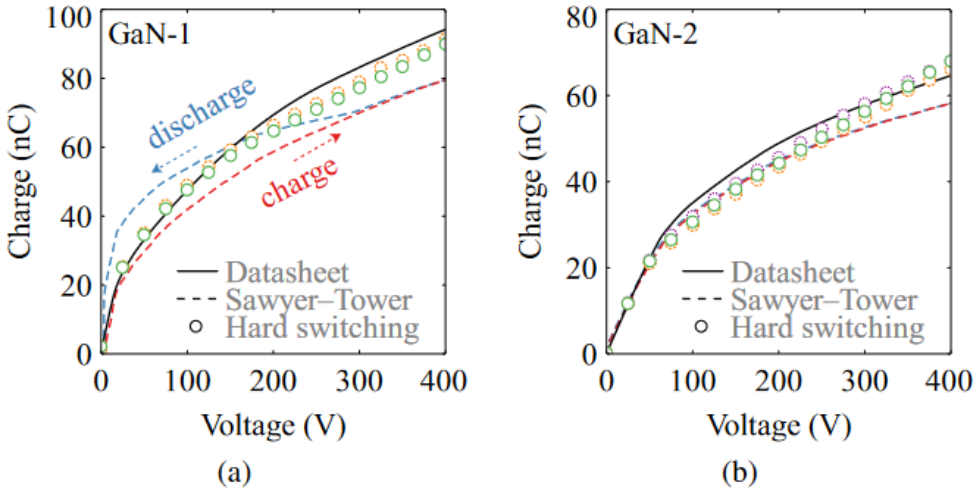


Fig. 26 Experimental QV curves obtained using the proposed hard-switching method (marked by circles) for two different GaN HEMT device types, where f_{sw} = 100 kHz, d = 0.5 and T_d = 100 ns. Results are also compared with curves based on datasheets and Sawyer–Tower method. To show that the results are repeatable, a device-sampling was carried out for (a) two pairs (solid and dashed circles) of GaN-1 devices with R_{GH} = R_{GL} = 47 Ω, and (b) three pairs (solid, dashed, and dotted circles) of GaN-2 devices with R_{GH} = 10 Ω and R_{GL} = 1 Ω. For both device types, the results for hard-switching follow the datasheet-based values quite closely.

Results for the two SiC devices (Fig. 27) indicate that the Q_O values in hard switching is considerably different in comparison to the datasheet values. Although the Sawyer-Tower measurements agree well with the datasheet curve for device SiC-2, it is not the case for device SiC-1. This shows that neither the small-signal curves nor the large-signal soft-switching curves can correctly predict the actual charge capacity for hard switching. To understand if this difference is due to any high-frequency effects, as hard switching is achieved at large dv/dt values, the switching speed was decreased for device SiC-2 by increasing the R_{GH} value up to two orders of magnitude as Fig. 27b shows. The corresponding v_{DS} waveforms are given in Fig. 27c, where the slowest speed (for R_{GH} = 4.3 kΩ) corresponds to charge and discharge times of ≈ 5 μs each, which matches in frequency for a 100-kHz excitation in the Sawyer–Tower circuit. The results indicate that Q_O stays unchanged with switching speed. One possible explanation of this lies in the topological difference between hard-switching and Sawyer–Tower circuits. In the former, C_O is allowed a considerable fully-off state after the transient (where v_{DS} is settled at V_{dc}), which allows the stored charge to settle to the dc electric field created by V_{dc}. In the latter on the other hand, the off-state voltage is continuously changing and a flat top in v_{DS} is never achieved, and the charges are subjected to a time varying electric field; this might create a different overall charge capacity in C_O.

For the Si-SJ devices (Fig. 28), the Q_O values in hard switching are significantly larger in comparison to the datasheet values beyond the knee-point voltages (marked by squares). The Sawyer-Tower curves lie close to the hard-switching curves, indicating that the large-signal behavior of C_O is considerably different to datasheet values. This observation is in agreement with the works by Zulauf et al. [20], [30], where the Sawyer–Tower measurements showed considerable discrepancies for Q_O, in comparison to datasheet values. Our results further indicate that the hard-switching charge capacity in Si-SJ devices could vary from the Sawyer–Tower curves as can be observed for device Si-2.

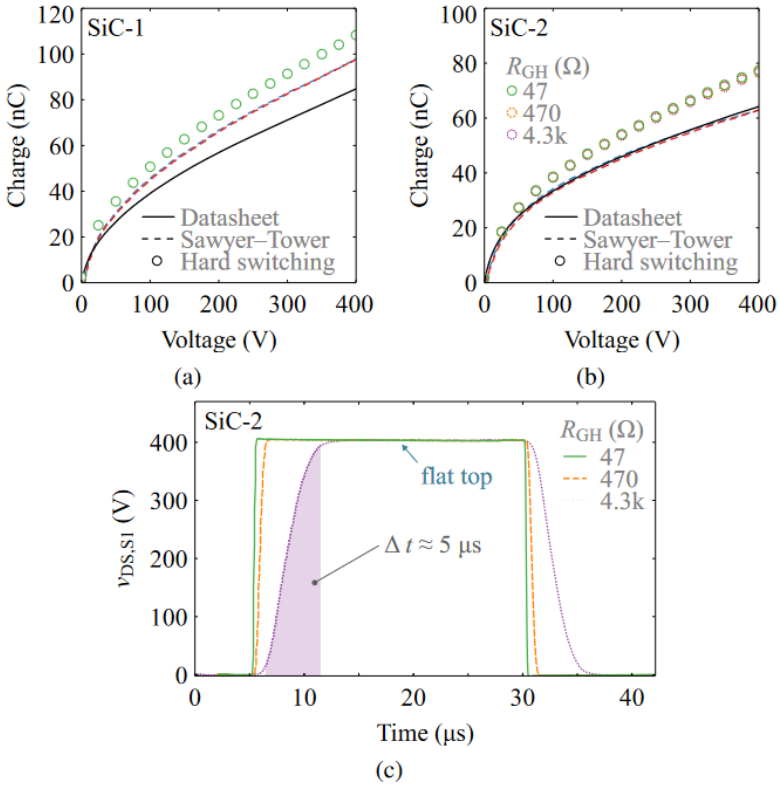


Fig. 27 Experimental QV curves obtained using the proposed hard-switching method for two different SiC device types: under the conditions (a) f_{sw} = 100 kHz, d = 0.5, T_d = 100 ns, R_{GH} = 47 Ω and R_{GL} = 1 Ω; (b) f_{sw} = 20 kHz, d = 0.5, T_d = 2 µs and R_{GL} = 1 Ω. For device SiC-2, the switching speed in hard switching was varied by changing R_{GH}: 47 Ω (solid circles), 470 Ω (dashed circles) and 4.3 kΩ (dotted circles). The results show that the QV curves exhibit no dependence on switching speed. The slowing down of the switching speed with increasing R_{GH} can be seen in (c) the v_{DS} waveforms.

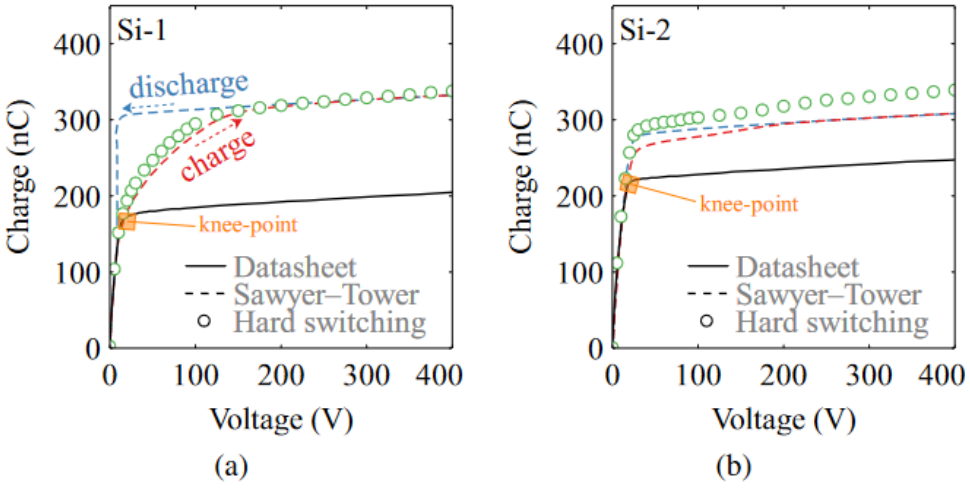


Fig. 28 Experimental QV curves obtained using the proposed hard-switching method for two different Si-SJ device types are compared with respective curves based on datasheets and Sawyer–Tower method. The conditions are: d = 0.5, T_d = 100 ns, R_{GH} = 47 Ω and R_{GL} = 1 Ω. A low f_{sw} of 20 kHz was used to keep the power dissipations in the devices low as the Si-SJ devices have much larger Q_o values (≈ 300 nC at 400 V).

As datasheet values could differ from the tested batch of devices, small-signal CV measurements on five samples of each device type were performed. The measured small-signal output charge values for each transistor, normalized with respect to their corresponding datasheet values, are plotted in Fig. 29. All devices are contained within a 10 % variation from datasheet values, apart from device Si-1, which shows a 20 % variation. The results for the samples of the GaN devices and device SiC-2 stay very close to their datasheet values.

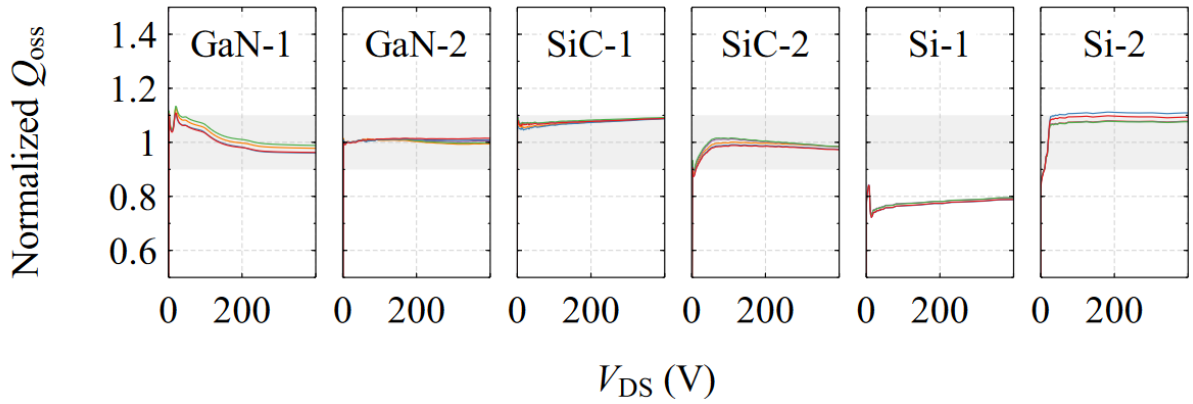


Fig. 29 Small-signal measurement results showing normalized Q_{oss} values (measured/datasheet) for a dc sweep of V_{DS} = 0 to 400 V. Five samples of each tested device-type were measured with a Keysight B1505A curve tracer at an excitation frequency of 100 kHz. The light-grey areas correspond to a ± 10 % variation from the datasheet values.

Fig. 30 compares $E_{on\text{-}Co}$ at 400 V for the tested devices, evaluated using the small-signal methods (datasheet and measured) and the hard-switching method (measured). For the two GaN-devices, all three methods show good agreement with differences contained within 5 %. On the other hand, for example, device SiC-2 shows a 21.1 % difference between datasheet and measured hard-switching values, which translates to a 0.211 × 25.56 μJ = 5.39 μJ difference in energy loss; and at a f_{sw} of 200 kHz, this means an additional power loss of 1 W, which is not negligible. The devices Si-1 and Si-2 show significant differences around 64.9 % and 35.6 % between methods 1 and 3, which cannot be explained even by the measured small-signal values. These results reveal two very important aspects about the large-signal behavior of Q_o in hard switching:

1) highly dependent on the semiconductor technology and the structures used within a given technology.
2) for certain devices, it cannot be predicted correctly with either the datasheet, or the large-signal curves related to soft-switching operation.

Datasheets should provide large-signal QV curves, and E_{on} should be separated into two parts to distinguish between the effects of C_O and load current.

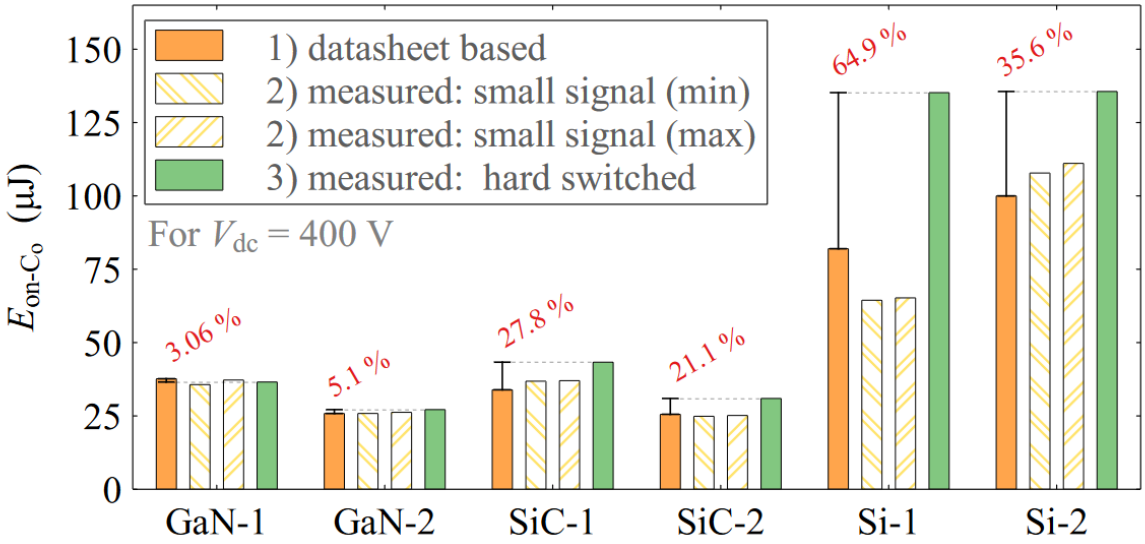


Fig. 30 Comparison of measured (hard-switching method) and datasheet-based $E_{on\text{-}Co}$ at 400 V for the devices studied in this work. $E_{on\text{-}Co}$ based on the small-signal measurements are also shown (only the cases with lowest and highest Q_{oss} values are included). The percentage differences between the datasheet and measured hard-switching results are not negligible for SiC and Si-SJ devices. This directly affects the accuracy of E_{on} as $E_{on\text{-}Co}$ is a load-independent contribution.

3. ON-State Losses: Dynamic R_{ON} Degradation

GaN HEMTs often suffer from dynamic ON-resistance (R_{ON}) degradation, where R_{ON} increases right after the device turn-on due to electron trapping phenomena. Electrons can get trapped either in the buffer and/or on the surface under high electric fields during the OFF-state [36], [37], and during hard-switching transients (as hot-electron trapping [38]). This results in higher conduction losses and has been a major concern in GaN power switching.

Most of the measurement methods found in the literature to characterize dynamic R_{ON} are based on different forms of pulsed measurements, e.g., with a single pulse stress [39], double pulses [40-44], and multiple pulses [41-43]. In these methods, a short test time (in the range of µs) is applied to avoid self-heating, as temperature also has an effect on the R_{ON} increase. However, results for identical devices are often very different and even sometimes conflicting in these studies. Fig. 31 compares the dynamic R_{ON} values from the literature with different measurement techniques applied to an identical GaN device (GS66508B/T) under hard-switching conditions. Large discrepancies in the dynamic R_{ON} increase can be observed, e.g., from 7% to 55% at an OFF-state voltage ($V_{ds(OFF)}$) of 400 V. Furthermore, results in [41] show a monotonic dependence on $V_{ds(OFF)}$ while those in [39] and [40] show a non-monotonic voltage dependence. These discrepancies could be attributed to the short test time, as it was observed that the trapping-related carrier transport time constants in the buffer can be on the order of seconds [36], [37], [43]. Insufficient test time fails to capture effects from any possible large trapping time constants, which, however, are seen in steady-state operations. Another factor that may give rise to the reported dynamic R_{ON} variations is the OFF-state bias time before pulsed tests, which may induce extra OFF-state trapping but is not always described, e.g., in [39] and [40] but not in [41]. These pre-stress conditions, nevertheless, are not representative of real power converter operations at steady-state.

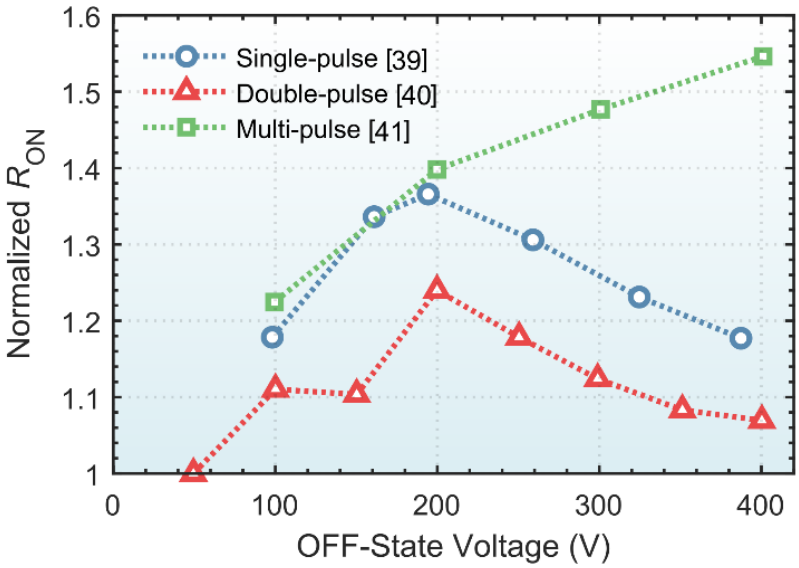


Fig. 31 Previously reported dynamic R_{ON} for an identical GaN HEMT (GS66508B/T) under hard-switching conditions. Significant discrepancies in dynamic R_{ON} values and behaviors can be observed.

Without consistent measurements, the significance of dynamic R_{ON} degradation remains unclear and a fair comparison between different GaN technologies is impossible. So far, only very few studies applied steady-state approaches to evaluate dynamic R_{ON}, e.g., in a Buck converter [36]. However, a full-power converter exhibits significant device losses and rises in device temperature, which also have an effect on R_{ON}. Therefore, distinguishing trapping-related time constants from thermal time constants in these methods is very challenging. This is important as studies in [43] and [44] show that the behavior of dynamic R_{ON} versus $V_{ds(OFF)}$ can vary significantly with temperature, which might be a source of inconsistencies when comparing different devices if the temperature is not controlled and unknown.

In this section, we show that some commercial GaN devices exhibit very slow transients before the dynamic R_{ON} stabilizes (up to 3 mins), and we reveal that insufficient test time can lead to spurious results and contradictory conclusions. These findings are enabled by our proposed steady-state method using a hard-switching half-bridge with an active measurement circuit, which minimizes device losses and temperature rise even with steady-state operations. This work highlights the need for steady-state measurements to accurately characterize the dynamic R_{ON} of GaN devices and provide a pathway toward a clearer identification and a fair comparison of dynamic R_{ON} between different technologies.

3.1. Methodology

3.1.1. Operation Principles

Fig. 32a illustrates the proposed circuit for investigating the dynamic R_{ON} degradation at steady-state. The low-side device Q_2 in the half-bridge circuit is the device-under-test (DUT). Instead of using an inductive or resistive load current I_L to measure R_{ON} when Q_2 is on, a measuring current I_m is injected from the active measurement circuit during the ON-time. Detailed operation modes are shown in Fig. 32b. Before switching, Q_2 is kept on and its static dc ON-resistance (R_{dc}) is examined to ensure that there is no residual trapping effect from previous tests. Then after t_0, Q_1 and Q_2 start to switch complementarily in continuous mode at a switching frequency of f_{sw}. Within one period, Q_2 is biased with V_{dc} during the OFF-state (t_2-t_4) and then experiences a hard turn-on event (t_4-t_5). During the hard-switching transient, the channel current i_{ch2} of Q_2 reaches its peak I_{pk}, which is considerably high due to the fast discharging of the DUT output capacitance and charging of the output capacitance of Q_1.

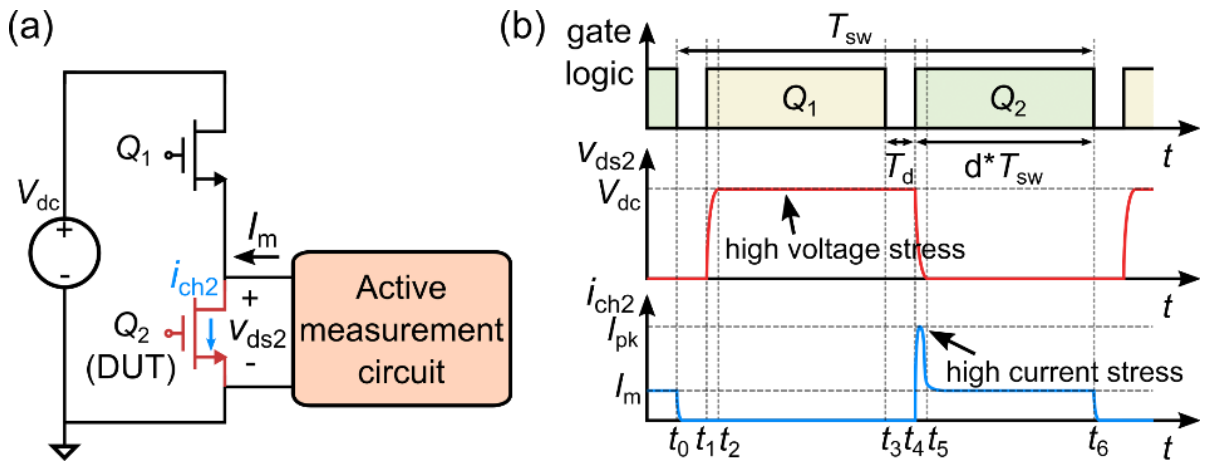


Fig. 32 (a) Schematic of the proposed half-bridge no-load circuit with the low-side transistor Q_2 as the device-under-test (DUT). A measuring current (I_m) is injected from the active measurement circuit to monitor the ON-state voltage of the DUT. (b) Gate control signals of the half-bridge and related waveforms of the drain-source voltage (v_{ds2}) and channel current (i_{ch2}) of the DUT. Q_1 and Q_2 are switched complementarily at steady-state. The R_{ON} of Q_2 is measured during t_5-t_6 immediately after the hard-switching transient (t_4-t_5).

This operation mode imposes high voltage and high switching current stress on the DUT, allowing one to investigate the effect of both OFF-state trapping and hot-electron trapping on dynamic R_{ON} degradation. On the other hand, the no-load circuit features minimal device losses and temperature rises even at steady-state. The hard-switching losses (P_{sw}) can be modeled as a quadratic function of the external load current I_L [47] as

$$P_{\mathrm{sw}} = (a + bI_{\mathrm{L}} + cI_{\mathrm{L}}^2)f_{\mathrm{sw}}$$

where $a = Q_{\mathrm{o}}V_{\mathrm{dc}}$ with Q_o the device output charge, and b and c are switch-dependent coefficients. By operating at no-load conditions (I_L = 0), switching losses are minimized and conduction losses (P_{con}) are only induced by the measuring current I_m, which is much smaller than with external load current. Assuming negligible gate losses, the total losses (P_{total}) of the DUT can be derived as follows

$$P_{\mathrm{total}} = P_{\mathrm{con}} + P_{\mathrm{sw}} = \; d\, I_m^2 R_{\mathrm{ON}} + Q_{\mathrm{o}}V_{\mathrm{dc}}f_{\mathrm{sw}}.$$

where d is the duty cycle of the DUT. Device losses can be further reduced with a low f_{sw}. By minimizing the device temperature rise, the R_{ON} increase is solely due to the trapping effect, which can be distinguished from thermal effects.

Moreover, this measurement method is independent of the type of load, which can reveal some intrinsic R_{ON} degradation from the devices, regardless of the type of load used. It also offers a possibility to independently investigate the additional degradation that different loads might induce in GaN devices.

3.1.2. Design of the Active Measurement Circuit

Here we revisit the design of ON-state voltage measurement circuits (OVMC) and propose an active measurement circuit to implement the measurement concept.

In principle, an OVMC blocks the high OFF-state voltage and allows measuring the ON-state voltage of the DUT with high resolution, soon after the switching transient. Diode-type clamping circuits have been widely used because of the low parasitic capacitance of the blocking diode [39]-[41], [44]. Typically, the diode forward current, which also flows to the DUT, is tuned to be small (e.g., ~20 mA) to avoid heating up the blocking diode, because the measurement accuracy relies on offsetting the diode forward voltage, but unfortunately, this parameter is temperature-dependent. Researchers have also proposed to use a second diode and achieve diode voltage drop compensation with an operational amplifier (op-

amp) [36], [37], but still, it is challenging to maintain an even temperature distribution and a voltage match for the diodes.

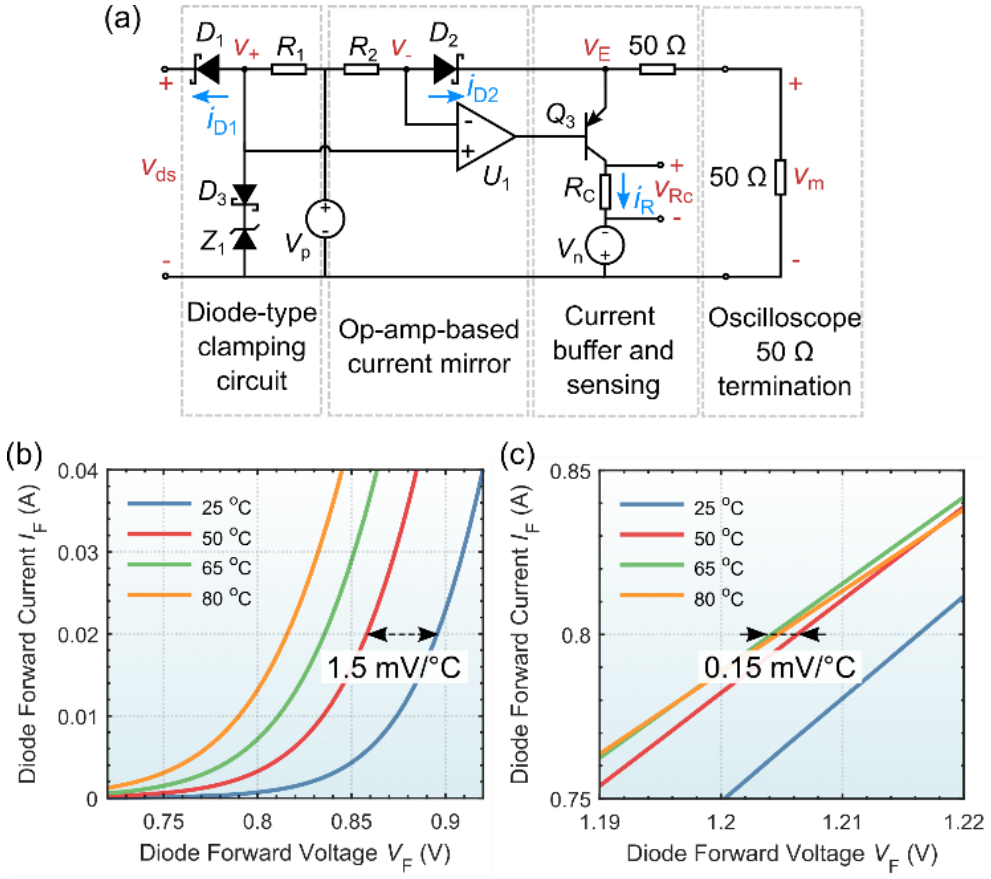


Fig. 33 (a) Schematic of the active measurement circuit featuring OFF-state voltage blocking, diode voltage compensation, current sensing, and 50 Ω output impedance. The blocking diode (i.e., D_1) shows significantly different temperature-dependent forward characteristics: (b) at low current levels (~20 mA): 1.5 mV/°C and (c) at high current levels (~800mA): 0.15 mV/°C.

By leveraging insights from prior work [41], [46], [48], we propose an active measurement circuit as shown in Fig. 33a to address the above-mentioned challenges. D_1 and D_2 are two identical SiC Schottky diodes (GB01SLT06-214). When the DUT is turned off, D_1 blocks the OFF-state voltage and v_+ is clamped by the clipping branch made of a low-voltage Schottky diode D_3 (SS12) and a Zener diode Z_1 (1SMA5913BT3G). When the DUT is turned on, the diode forward current i_{D1}, which also goes through the DUT, is designed to be considerably higher than in existing clamping circuits, e.g., around 800 mA with V_p = 3.3 V and R_1 = 2.5 Ω. Diode voltage compensation is achieved by the feedback control of a high-speed op-amp U_1 (AD8045) to achieve $v_- = v_+$ and by having $R_2 = R_1$ as discussed in [38]. Therefore, $i_{D2} = i_{D1}$, and from symmetry, we obtain $v_E = v_{ds}$. The ON-state voltage of the DUT is then measured by the 50 Ω termination of the oscilloscope input as

$$v_{ds} = v_E = 2v_m .$$

To handle the large current i_{D2} in the Op-amp-based current mirror, we incorporated a current buffer that consists of a PNP bipolar junction transistor Q_3 (PBSS5240X), a sensing resistor R_C = 3.3 Ω, and a voltage source V_n = 3.3 V. The collector current i_R of Q_3 is identical to the diode currents as the base current of Q_3 and the current into the oscilloscope input are negligible. Therefore, the injected current into the DUT can be monitored by measuring v_{Rc} as

$$i_{DUT} = i_{D1} = i_{D2} = i_R = \frac{v_{Rc}}{R_C},$$

and the real-time R_{ON} can be calculated as follows

$$R_{\mathrm{ON}} = \frac{v_{\mathrm{ds}}}{i_{\mathrm{DUT}}} = \frac{2v_{\mathrm{m}}R_{\mathrm{C}}}{v_{\mathrm{Rc}}}.$$

The proposed measurement method only relies on two simple voltage measurements, v_m and v_{Rc}. The *I-V* characteristics of diodes are only measured once to find two diodes (D_1 and D_2) exhibiting the closest voltage drop. This method eliminates the need for diode voltage drop offsetting in postprocessing since voltage compensation is implemented in real-time measurements.

By tuning the operation point at higher current levels, the diode voltage drop is much less sensitive to temperature variances as shown in Fig. 33b and Fig. 33c. For example, the temperature coefficient of the SiC Schottky diode used is 1.5 mV/°C at 20 mA and 0.15 mV/°C at 800 mA measured with a B1505 semiconductor analyzer. Hence a much better diode voltage match and compensation can be achieved. Also, a high forward current accelerates the discharge of the diode parasitic capacitance during the turn-on transient and thus enables fast transient responses.

3.1.3. Validation with Si MOSFET

The proposed method also benefits from the 50 Ω output impedance, which provides impedance matching with cables and 50 Ω input termination of the oscilloscope. This is important because it allows a flat gain for all the frequency responses, minimizes signal reflection, and presents the least settling effect. Conventional voltage clippers use high input impedance voltage probes (e.g., TPP1000 1 GHz passive probe from Tektronix), which exhibit undesirable long settling time that may be misinterpreted as dynamic R_{ON} degradation effects, even when testing a Si MOSFET.

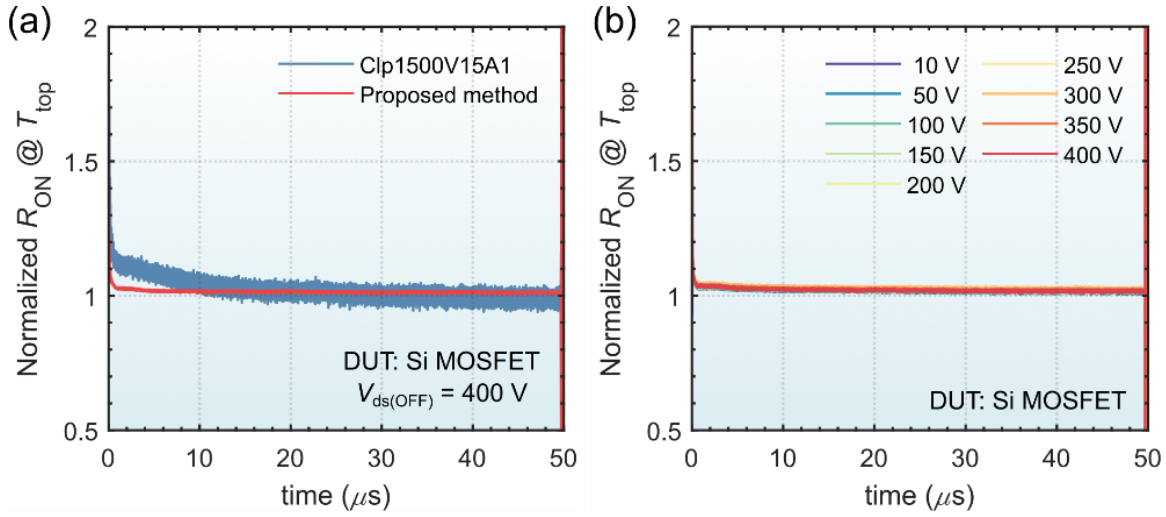


Fig. 34 Time-resolved waveforms of R_{ON} normalized to $R_{dc}(T_{top})$ of the Si DUT under steady-state conditions, with f_{sw} = 10 kHz, d = 50%, $V_{g(ON)}$ = 10 V, $R_{g(ON)}$ = 47 Ω. (a) Comparison between a commercial voltage clipper (Clp1500V15A1) and our proposed method. The former exhibits a settling time in the range of 10 μs, which limits its use at higher frequencies. (b) Normalized R_{ON} waveforms at different OFF-state voltages for the Si DUT, confirming no degradation in dynamic R_{ON} for all blocking voltages, as expected.

In order to verify and justify our method before testing GaN HEMTs, we used a bottom-side cooled Si MOSFET (STL26N60DM6, 600 V/15 A) to benchmark our method, and compare the results with a commercial voltage clipper (Clp1500V15A1). The test conditions were as follows: switching frequency f_{sw} = 10 kHz, duty cycle d = 50%, gate drive voltage $V_{g(ON)}$ = 10 V, and gate turn-on resistor $R_{g(ON)}$ = 47 Ω. The results were normalized to the R_{dc} obtained from 4-wire dc measurements at the corresponding top surface temperatures (T_{top}), which were monitored with an infrared camera (Fluke TiS65). Fig. 34a shows that the commercial voltage clipper suffers from a long settling time and low resolution, mainly due to

the use of high-impedance termination and large vertical division setting of the oscilloscope. The long settling time, in the range of 10 μs, limits its use at higher switching frequencies, while the proposed method shows nearly zero settling time and higher resolution thanks to 50 Ω matching impedance. Fig. 34b shows the expected absence of dynamic R_{ON} degradation at different $V_{ds(OFF)}$ for the Si DUT and reveals the high fidelity of the measurements, validating our method.

3.2. Dynamic R_{ON} Measurements: Multiple Pulses Are Not Enough

The proposed method was used to investigate the dynamic R_{ON} behavior of a commercial Schottky-type *p*-GaN gate HEMT (GS66502B, 650 V/7.5 A) at steady-state. The GaN DUT is bottom-side cooled and its top surface temperature T_{top} was monitored. Instead of studying the effect of temperature on dynamic R_{ON} degradation, here we aimed to exclude the temperature effects since temperature rises also have an effect on the R_{ON} increase and dynamic R_{ON} versus $V_{ds(OFF)}$, as shown in [36], [43], and [44]. We first chose a low switching frequency, i.e., 10 kHz, that led to negligible switching losses, and measured T_{top} remained almost unchanged (26 °C – 27 °C) for all $V_{ds(OFF)}$ at steady-state. In this way, the dynamic R_{ON} increase, due solely to electron trapping, can be measured and trapping-related time constants can be distinguished from other effects.

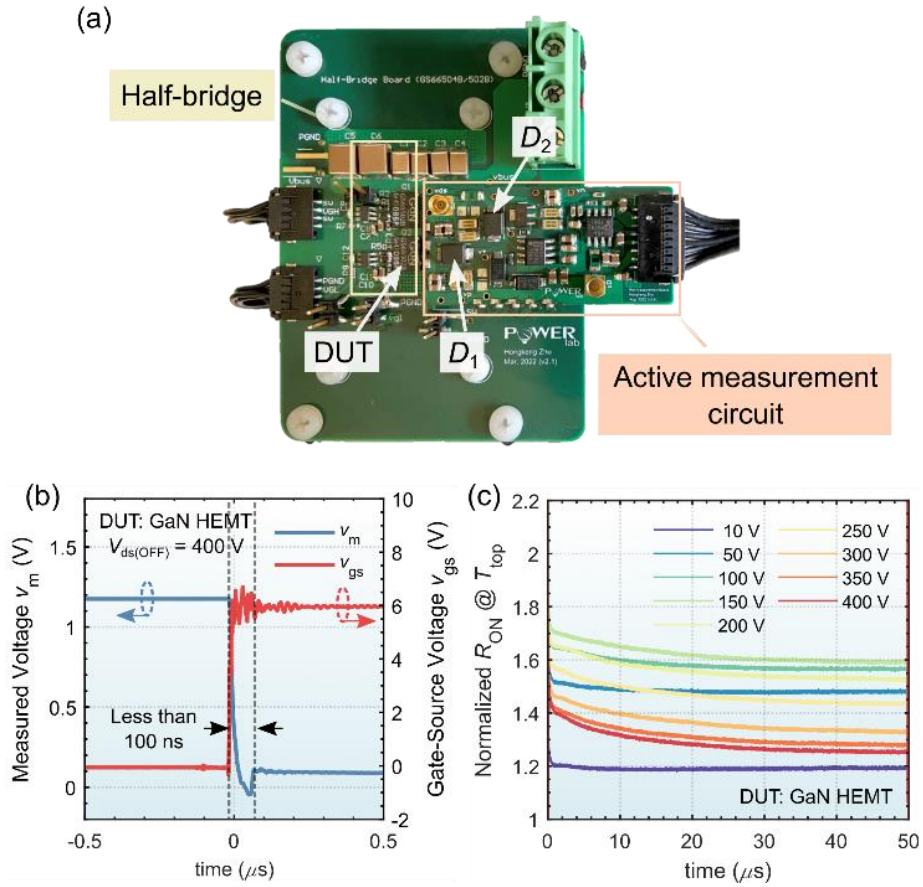


Fig. 35 (a) Hardware implementation of the half-bridge circuit board with the GaN DUT and the active measurement circuit. (b) Dynamic response of the measurement circuit when testing with the GaN DUT. v_m quickly settles in less than 100 ns before the ON-state voltage is monitored. (c) Time-resolved waveforms of the dynamic R_{ON} normalized to $R_{dc}(T_{top})$ of the GaN DUT under steady-state conditions at different $V_{ds(OFF)}$, with f_{sw} = 10 kHz, d = 50%, $V_{g(ON)}$ = 6 V, $R_{g(ON)}$ = 10 Ω. At such conditions, the steady-state temperature of the DUT remains substantially unchanged (26 °C – 27 °C) because of the negligible switching and conduction losses.

Fig. 35a shows the half-bridge circuit with the GaN DUT and the active measurement circuit, mounted close to the DUT to minimize interconnection parasitics. Fig. 35b shows the dynamic response of the

measurement circuit where the measured voltage v_m quickly settles in less than 100 ns after the DUT is turned on. The fast dynamic response is crucial as GaN transistors are able to operate at high switching frequencies with a short ON-time for measurements. Fig. 35c shows the steady-state R_{ON} waveforms during the ON-time at different $V_{ds(OFF)}$ with f_{sw} = 10 kHz, d = 50%, $V_{g(ON)}$ = 6 V, $R_{g(ON)}$ = 10 Ω. Results are normalized to the R_{dc} at the corresponding T_{top}. From Fig. 35c, it can be seen that the investigated GaN DUT exhibits a notable increase in dynamic R_{ON} with $V_{ds(OFF)}$, which peaks between 100V and 200V. A de-trapping pattern during the first 40 μs of the ON-time starts to appear when $V_{ds(OFF)}$ > 50 V and becomes more obvious with higher $V_{ds(OFF)}$. Interestingly, there is a considerable increase of 20% in R_{ON} even at $V_{ds(OFF)}$ = 10 V. This could be attributed to gate-stress-induced V_{th} shift [39], and/or buffer trapping which is also observed at a low OFF-state voltage $V_{ds(OFF)}$ = 25 V [37].

These new findings for this type of GaN device can only be captured at steady-state due to large trapping time constants that were observed on the order of 1 – 100 s. To put it in perspective, real-time R_{ON} waveforms were recorded before, during, and after switching at 10 kHz for a period of 5 mins with $V_{ds(OFF)}$ = 100 V and 400 V respectively as shown in Fig. 36a and Fig. 36b. A low sample rate of 50 kS/s and high-resolution mode were chosen to visualize the real-time R_{ON} evolution on the oscilloscope screen during a monitor window of 10 mins. The bottom contour of the waveforms during switching (from t = 0 s to t = 300 s in Fig. 36) depicts the evolution of R_{ON} while the DUT is switched on. A long voltage-dependent transient is observed before R_{ON} stabilizes (after which no substantial change in R_{ON} can be observed any longer), i.e., ~ 3 mins at $V_{ds(OFF)}$ = 100 V and ~ 10 s at $V_{ds(OFF)}$ = 400 V. It is also interesting to notice that after stopping switching and permanently turning on the DUT (after t = 300 s in Fig. 36), it still takes a long time for R_{ON} to recover back to the static R_{dc} value (which is also $V_{ds(OFF)}$ dependent). During the whole monitor window of 10 mins, the device temperature variance was small (< 4 °C) and therefore self-heating effect could be excluded, which is not possible with conventional inductive or resistive loaded circuits, e.g., Buck converters.

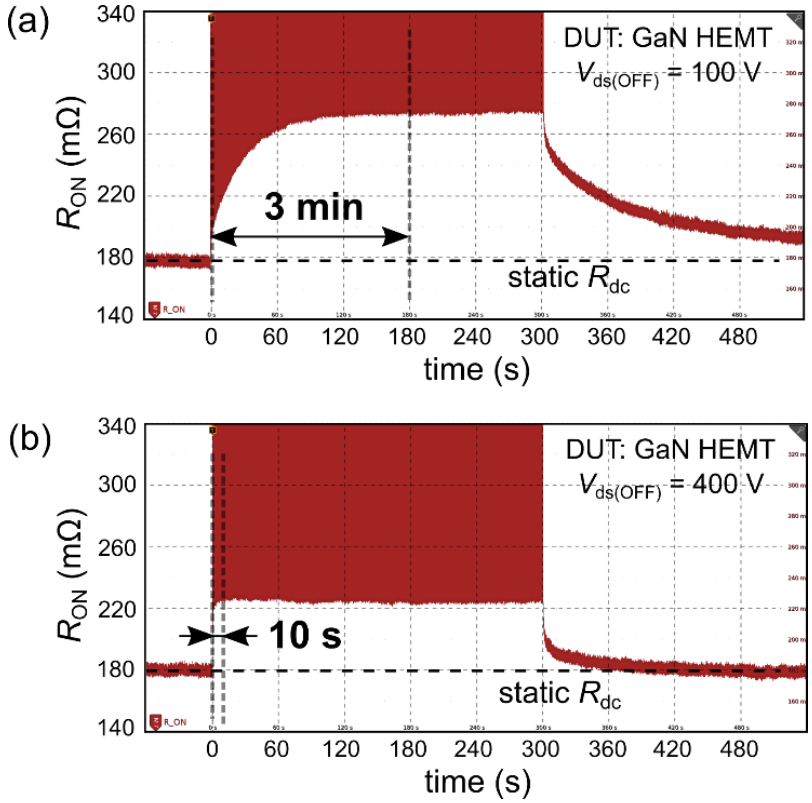


Fig. 36 Real-time monitoring of the dynamic R_{ON} before, during, and after switching at 10 kHz from t = 0 s for 5 mins at (a) $V_{ds(OFF)}$ = 100 V, and (b) $V_{ds(OFF)}$ = 400 V. Heating is not responsible for the transients before R_{ON} stabilizes as the temperature variance is small (< 4 °C) within the measurement window of 10 mins. Significant trapping and de-trapping time constants can be observed.

The slow transient responses in Fig. 36 suggest that results from multi-pulse tests (typically < 1 ms) are not representative of the dynamic R_{ON} behaviors at steady-state. To confirm this, we also performed multi-pulse tests for the same DUT at 10 kHz for a total test time ranging from 10 ms to 1 min, which is equivalent to a number of pulses from 100 to 6×10^5. Again, the self-heating effect is negligible thanks to the no-load operation at a low switching frequency. The averaged R_{ON} computed for the last pulse is shown in Fig. 37 and compared to steady-state results measured after operating for more than 3 mins. As can be seen, the time required for the dynamic R_{ON} to stabilize depends on $V_{ds(OFF)}$, with R_{ON} approaching the steady-state values more slowly for the lower voltage range ($V_{ds(OFF)}$ < 200 V) than for the higher voltage range.

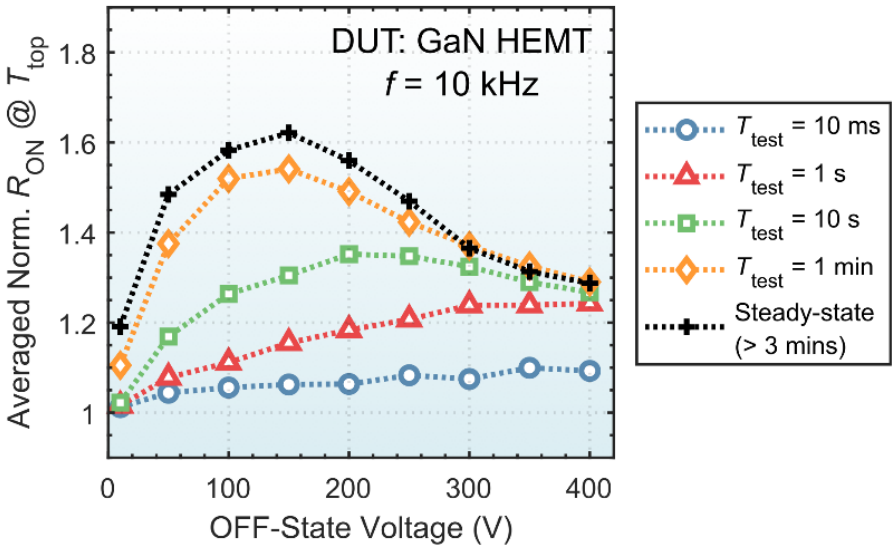


Fig. 37 Averaged normalized R_{ON} over the ON-time of the last pulse in multi-pulse tests at 10 kHz for a total test time ranging from 10 ms to 1 min, the number of pulses being from 100 to 6×10^5. Multi-pulse tests with an arbitrary test time are not able to accurately capture the dynamic R_{ON} behaviors at steady-state and may lead to wrong conclusions such that dynamic R_{ON} barely exists.

Although the number of pulses applied here is much larger than in typical multi-pulse tests, these results can still lead to spurious conclusions if the dynamic R_{ON} has not yet stabilized. For example, with a test time of 10 ms, one may conclude that dynamic R_{ON} barely exists, and with a test time of fewer than 1 s, one cannot capture the partial recovery pattern at high voltages (Fig. 37).

This could explain the monotonic voltage dependence observed for GaN devices from the same manufacturer in [41] and [42], which only applied a few hundred pulses and performed measurements before the dynamic R_{ON} stabilized. Also, in Fig. 36 and Fig. 37, we did not apply any pre-stress time and the DUT was fully relaxed before tests to ensure consistent measurements and comparisons. This is not always practiced in pulsed measurements and could lead to conflicting results. Results in Fig. 36 and Fig. 37, clearly highlight the need for steady-state methods for accurate measurements of dynamic R_{ON}, and more importantly, raise awareness of these inconsistencies from pulsed measurements. With a consistent measurement method, we also evaluated dynamic R_{ON} at higher switching frequencies at steady-state and studied its effect, which can be used to predict the device conduction losses in real-circuit applications.

Fig. 38a shows the averaged R_{ON} values over the ON-time at different switching frequencies and $V_{ds(OFF)}$ along with the corresponding T_{top} in Fig. 38b. An increase in R_{ON} with frequency is observed, which directly correlates to the relaxation pattern during the ON-time (Fig. 35c) and the reduced relaxation time at higher frequencies. More remarkably, the dynamic R_{ON} shows a non-monotonic dependence on $V_{ds(OFF)}$, which peaks at around 150 V with an increase of 60% – 80% and partially recovers to 30% – 40% at 400 V. This behavior concurs well with device physics models ascribing the recovery to an increased hole flow that can partially neutralize trapped electrons, by buffer leakage [35] and/or by enhanced impact ionization under high electric fields [37].

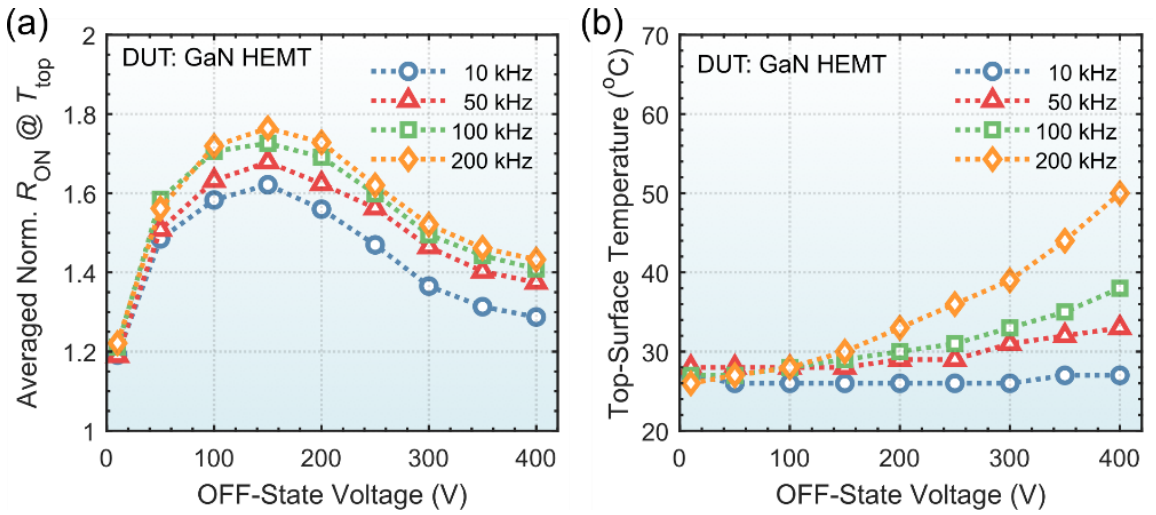


Fig. 38 (a) Averaged normalized R_{ON} of the GaN DUT over the ON-time at different switching frequencies and OFF-state voltages. (b) Top-surface temperature of the DUT measured under steady-state conditions.

It should be noted that in this letter the dynamic R_{ON} of the GaN DUT was characterized only under hard-switching operations. However, the proposed measurement concept and the active measurement circuit are very general and could also be used in soft-switching applications, where GaN devices can be operated at higher switching frequencies and the effect of hot-electron trapping can be essentially excluded from OFF-state trapping.

The proposed method enabled the observation of slow and voltage-dependent transient response of dynamic R_{ON} in the tested type of GaN device, and can also be applied to test the stabilization time of dynamic R_{ON} for other devices. Other types of GaN devices may behave differently in terms of dynamic R_{ON} degradation, but this work raises awareness of the effect of poorly measured dynamic R_{ON}, as illustrated in Fig. 1 and in our multi-pulse tests (Fig. 37), and highlights that steady-state methods should be applied for accurate measurements to predict their performance in real power converter operations.

4. Conclusions

This report proposes ways to measure device characteristics to highlight the impact of different WBG technologies on the device efficiency as well as converter efficiency and integration. In particular, we have discussed different methods for evaluating the OFF-state and ON-state losses for power semiconductor devices used in switched-mode power electronics. These measurements are based on both electric methods as well as calorimeter-based methods to precisely capture losses even at high switching frequencies.

It is outlined that in soft-switching, the C_O hysteresis losses during the charging and discharging of C_O define an upper limit for switching frequency. In general, WBG devices offer much better soft-switching performance. In hard-switching, the actual output charge Q_O that determines the C_O-related hard-switching losses cannot be predicted from datasheet curves for certain devices. It is suggested that manufacturers should include such information of soft-switching and hard-switching C_O losses in the datasheets. In terms of ON-state performance for GaN devices, we show that pulsed measurements with an arbitrary test time do not give an accurate picture of dynamic R_{ON} behavior. The proposed methods can be used to standardize measurements of losses in wide-bandgap devices, and benchmark different technologies, eventually support a proper promotion of WBG technologies.

5. Appendices

Here we provide some guidelines for efficiency measurements on a semiconductor level and standardization:

5.1. Appendix 1:

A. General guidelines for standardization

This report highlights important OFF-state and ON-state losses observed in power semiconductor devices used in switched-mode power electronics. Information about these losses are, in some cases, not available in datasheets, thus causing lower-than-expected converter efficiencies.

Unexpected C_O hysteresis losses, that occur during the charging and discharging of C_O, pose a limitation on the maximum switching frequency of the device. Although generally WBG devices offer much smaller soft-switching C_O hysteresis, it is observed that this effect is dependent on the device architecture. It is suggested that manufacturers include double-sweep capacitance-voltage measurements of the device, using the suggested methods in this report, for drain-source voltages varying from 0 to near the device maximum voltage rating. The dissipated energy extracted from the observed C_O hysteresis should be provided, which enables the estimation of soft-switching C_O hysteresis losses for a given switching frequency.

In hard-switching, it was observed that the output charge $Q_{O,}$ which determines the C_O-related hard-switching losses, cannot always be predicted correctly from the curves provided in datasheets or from large-signal curves (which are related to soft-switching operation). The output capacitance under hard-switching is highly dependent on the semiconductor technology and the structures used within a given technology. It is suggested that datasheets provide large-signal QV curves (using for example the energy-based method proposed in this report), and that E_{on} be separated into two parts to distinguish between the effects of C_O and load current.

In terms of ON-state performance for GaN devices, this report shows that pulsed measurements with arbitrary test times do not provide an accurate picture of dynamic R_{ON} behavior. The proposed method in this report enables the observation of slow and voltage-dependent transient responses of dynamic R_{ON} and can be applied to test the stabilization time of dynamic R_{ON} for GaN devices. This report raises awareness of the effect of poorly measured dynamic R_{ON}, and highlights that steady-state methods should be applied for accurate measurements to predict their performance in real power converter operations. It is suggested that a standardized, steady-state method is used to provide measurements of the dynamic R_{on} in the datasheets, under hard- and soft-switching.

In conclusion, the proposed methods in this report can be used to standardize loss measurements in wide-bandgap devices, to benchmark different technologies, which eventually support a proper promotion of WBG technologies.

B. Contribution to JEDEC guidelines

The research conducted in this work is already making an impact on the industry standards, as evidenced by its contribution to recent JEDEC discussions for new guidelines on these topics (unpublished). Specifically, the methodologies and findings concerning Coss losses in power devices detailed in this report are being considered to be incorporated into JEDEC's future guidelines. These discussions are being carried by two dedicated subcommittees within JEDEC: JC-70.1, focusing on GaN power electronics, and JC-70.2, which concentrates on SiC power electronics conversion semiconductor standards. These subcommittees are composed of leading industry specialists from across the globe, representing a diverse array of companies that specialize in power semiconductors, power supply production, and test equipment manufacturing. The inclusion of the procedures and recommendations proposed in this work in

such guidelines reflects a significant contribution to standardizing test methods for evaluating power device efficiency, underscoring the relevance and applicability of this research to current and future technological advancements in the field of power electronics.

5.2. Appendix 2: Guidelines for Soft-Switching Output Capacitance Loss Measurements

A guideline for evaluating the soft-switching output capacitance hysteresis losses using the Sawyer-Tower technique is provided as follows:

1. Prepare the experimental setup such as Fig. 39 including a signal generator, a high-voltage power amplifier, an oscilloscope, two passive voltage probes, and a circuit board with the DUT (always OFF) and a high-quality-factor reference capacitor. Cautions should be taken to deskew the voltage probes and validate the choice of reference capacitor;
2. Set up operation conditions (frequency, e.g., from hundreds of kHz to tens of MHz, and peak voltage, e.g., from 100 V to 400 V for 650 V rated devices);
3. Perform measurements and capture v_{in} and v_{ref} waveforms;
4. Calculate and obtain the charge-voltage (QV) curves at different test conditions;
5. Compute the soft-switching output capacitance losses (E_{diss}) from the obtained QV curves.

It is suggested that the manufacturers provide the soft-switching QV curves at a few test conditions in the datasheet, as well as the E_{diss}-f and E_{diss}-V characteristics. A calorimetric validation such as the one presented in Section 2.1.4 is also encouraged if available.

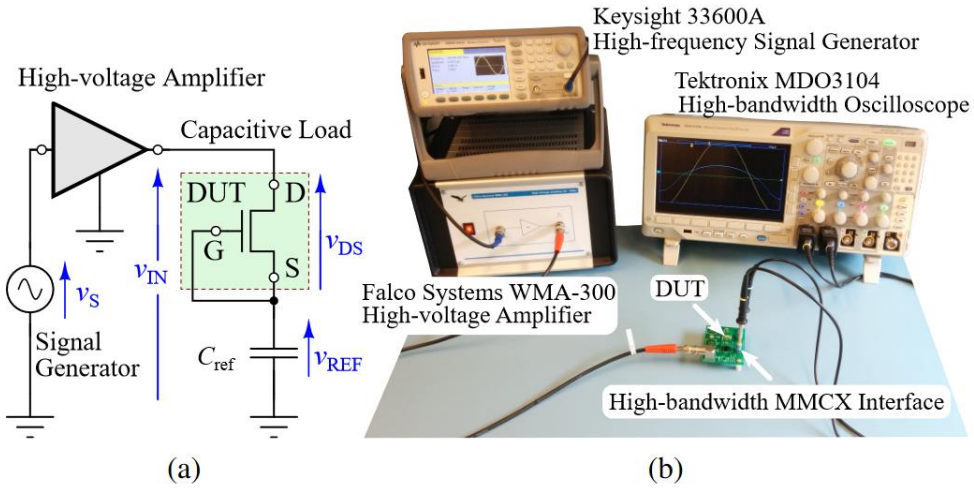


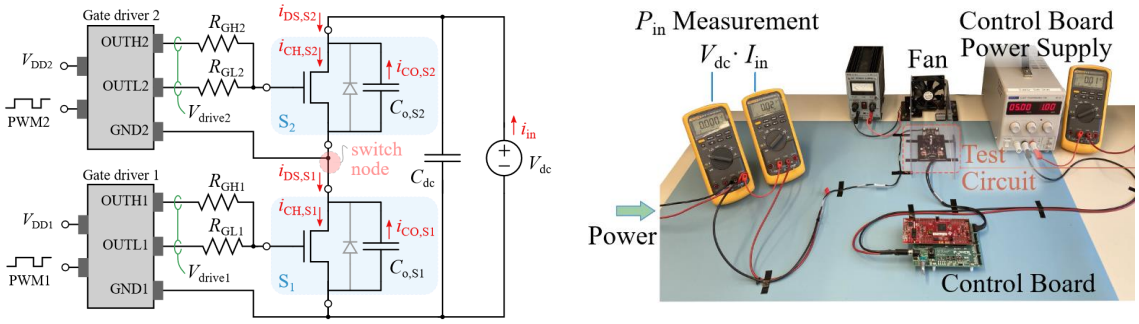
Fig. 39 (a) Schematic and (b) example of an experimental test setup of the Sawyer-Tower measurement technique used to analyze large-signal output capacitance under soft-switching conditions

5.3. Appendix 3: Guidelines for Hard-Switching Output Capacitance Loss Measurement

Large-signal behavior of output charge in hard switching cannot be accurately predicted by the small-signal CV curves in the datasheet for some devices. A guideline to characterize the hard-switching output capacitance losses is provided as follows:

1. Prepare a test circuit board including a half-bridge of two identical devices of interest and the gate driving circuits. Parasitic capacitance should be minimized such that a heat sink should not be used. Cautions should be taken on the choice of gate resistance to avoid false turn-on;
2. Prepare the experimental setup such as Fig. 40 including an input dc voltage source, a control board, two multimeters for input power measurements and a fan for air-cooling;

3. Set up the switching frequency f_{sw}, in the range of tens of kHz to avoid self-heating. Perform the measurements by sweeping the input voltage V_{dc} and measure the input power P_{in}.
4. Compute the output charge $Q_o = \frac{1}{2}\frac{P_{in}}{V_{dc} f_{sw}}$ and obtain the hard-switching QV curve.



(a) (b)

Fig. 40 (a) Schematic and (b) example of an experimental test setup of the no-load half-bridge technique to evaluate the large-signal QV curves under hard-switching conditions.

5.4. Appendix 4: Guidelines for Steady-State Dynamic On-Resistance Measurements

Dynamic on-resistance for some GaN devices can take several minutes to stabilize. A guideline to characterize the dynamic R_{on} of GaN devices at steady-state is provided as follows:

1. Build up the half-bridge circuit board with the DUT and the active measurement circuit, which is proposed in Section 3.1.2;
2. Set up operation conditions, including the switching frequency and OFF-state voltage;
3. Real-time dynamic R_{on} can be monitored on the oscilloscope screen with math operation. Wait for the dynamic R_{on} to stabilize before changing the test conditions. Monitor the device temperature at the same time;
4. Capture the time-resolved waveforms of dynamic R_{on} at each test condition and compute the average values during the ON-state. Obtain the normalized dynamic R_{on} of the GaN DUT at different switching frequencies and OFF-state voltages.

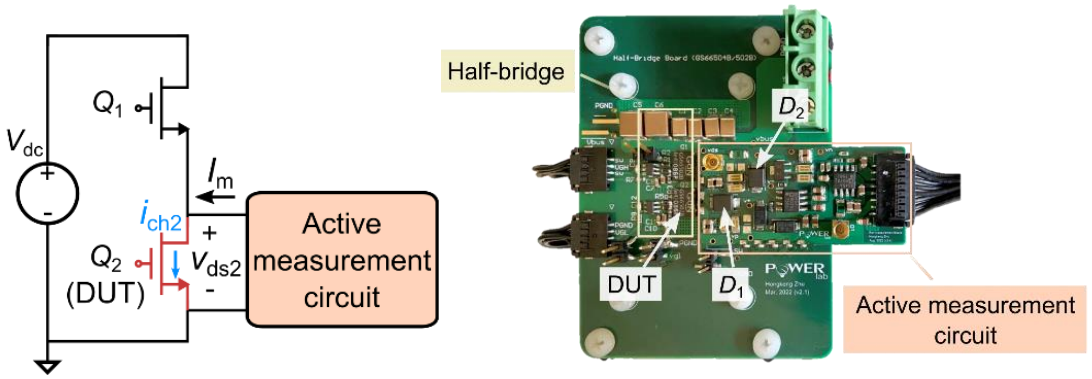


Fig. 41 (a) Schematic and (b) example of an experimental test circuit of the hard-switching half-bridge with active measurement circuit to accurately measure the dynamic ON-resistance at steady-state.

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